Phoenix

Phoenix microsystems, inc.
991 DISCOVERY DRIVE
HUNTSVILLE, ALABAMA 35806
TEL: (205) 721-1200 FAX: (205) 837-1256 TELEX: 752592

January 1, 1990

TO: Holder of the Model 5500A Instruction Manual, Revised 15 September 1989

SUBJ: Change 1

The enclosed is change 1 to the model 5500A instruction manual. This change is being made to update your manual to include new features added with the release of version 7.04 of the 5500A software. If you do not have version 7.04 or later, **do not** install this change.

To install this change, proceed as follows:

1. Remove pages 1–3 through 1–8 in section one of your manual.
2. Insert the new pages 1–3 through 1–8 into your manual. Make a pen and ink entry on the section one record of changes reflecting that change 1 has been effected.
3. Remove table of contents and pages 3–11 through 3–58 of section three of your manual.
4. Insert the new table of contents and new pages 3–11 through 3–58 into section three of your manual.
3. Remove the table of contents and pages 5–1 through 5–2 of section five of your manual.
4. Insert the new table of contents and new pages 5–1 through 5–2b into section five of your manual.
5. Remove the index from your manual and install the new index

Sincerely,

Dennis E. Crowley

LATA	Local Access and Transport Area
LBO	Line Build Out
LED	Light-Emitting Diode
PABX	Private Automatic Branch Exchange
PBX	Private Branch Exchange
PROM	Programmable, Read Only Memory
RAM	Random Access Memory
R&D	Research and Development
RFI	Radio Frequency Interference
ROM	Read-Only Memory
SNA	Systems Network Architecture
TMS	Transmission Measurement System
TelCo	Telephone Company
UPS	Uninterruptible Power Supply
WATS	Wide Area Telephone Service

1.5 INSTRUCTION BOOK

This Operating Manual contains information required to install, check and operate the Phoenix microsystems, inc. Model 5500A Communications Analyzer. It contains the following sections:

Introduction
Description
Installation
Operation
Parameter Descriptions
Remote/Printer Operation
Performance Monitoring
Maintenance
Options
Index

1.6 SPECIFICATIONS

The specifications for the Model 5500A are presented in Table 1-3.

Table 1-3. Model 5500A Specifications.

CHARACTERISTIC	SPECIFICATION
MODES OF OPERATION	
Emulation	Emulate DTE mode (for connection to DCE) Emulate DCE mode (for connection to DTE)
System Configuration	Full Duplex, Single Transmit, and Self Loop modes
Timing Modes	Synchronous, Asynchronous, and Recovered Timing
Framing Formats	Framed, Unframed, ESF, and SLC®96
TRANSMITTER	
Pattern Generator	
Fixed Patterns	MARK, SPACE, ALT, TSET ("10000" repeating), and TRESET ("100" repeating)
User-programmable	24 to 16,384-bit repeating pattern
Pseudorandom Patterns	63 (2^6-1), 511 (2^9 -1), SYSY 511, X25 511, 2047 (2^{11} -1), Reverse 2047, 2^{15}-1, 2^{20}-1, QRW, NET55, 2^9-1 A,
Messages	FOX message (ASCII), FOX 2 (in async 5-bit baudot, 6-bit EBCDIC, 7-bit ASCII, 8-bit BCDIC; in sync 8-bit ASCII)

Table 1-3. Model 5500A Specifications.
(Continued)

CHARACTERISTIC	SPECIFICATION
Message Format	Character Length - 5, 6, 7, or 8 bits (Async Timing), Parity - Odd, Even, or None, Number of Stop Bits - 1 or 2
Internal Data Rates (Synthesized)	50Hz - 500KHz @ + .1Hz increments 500KHz - 6.5MHz + 1Hz increments 6.5MHz - 13 MHz + 2Hz increments (with an accuracy of 1ppm @ 25°C; 5ppm @ 0°C to +50°C with an aging rate of 3ppm first year and 2 ppm/year thereafter.)
Data Inversion	Available for transmit and receive data
Error Insertion	Programmable from 5E-2 to 1E-9
Timing Sources	Internal Clock (see above rates), User Clock (rear panel connection), Interface Module
RECEIVER	
Receiver Timing	
Modes	Synchronous (1 x bit rate clock received through Interface Module for bit rates from 50 bps to 13 Mbps Asynchronous (16 x bit rate clock internally provided for bit rates from 50 bps to 64 Kbps) Recovered (1 x bit rate clock recovered from data transitions for bit rates from 75 bps to 48Kbps)
Data Error Analysis	
Modes	Single and Continuous
Acquiring Synchronization	MARK, SPACE, ALT, FOX, TISET, TIRSET0=24 + 32 = 56 BITS, SYS511, X25511 = ENTIRE PAT = 4088 BITS PSEUDO RANDOMS = 24 + 32= 56 BITS
Loss of Synchronization	Adjustable - Factory setting is bit error rate of 10-1 error/bit. User may set any rate between 8.96x10-1 and 1x10-3 errors/bit

Table 1-3. Model 5500A Specifications.
(Continued)

CHARACTERISTIC	SPECIFICATION
Bit Error Rate Tests	
Numeric Results Available (Interface Module Dependent)	Bit Errors, Bit Error Rate, Adjusted Bit Errors, Adjusted Bit Error Rate, Bit Count, Blocks CRC Errors, Burst Errors, CRC Error Rate, Current Bit Errors, Current Bit Error Rate, Errored Blocks, Error Free Blocks, Errored Block Rate, Frame Bit Errors, Frame Bit Error Rate, Number of Pattern Sync Losses, Power Failures, Receiver Bipolar Violations, Greater Than 15 Zeros Events, and Frame Sync Losses
Time Dependent Results (Interface Module Dependent)	Blue Alarm Seconds, Burst Errors, CRC Errored Seconds, CRC Error Free Seconds, Elapsed Days, Error Free Seconds, Errored Seconds, Errored Second Rate, Elapsed Time, Elapsed Time in Seconds, Frame Loss Seconds, Frame Bit Errored Seconds, Frame Bit Error Free Seconds, Receiver Bipolar Violation Free Seconds, Receiver Bipolar Violation Rate, Receiver Bipolar Violation Seconds, Sync Loss Seconds, Transmitter Bipolar Violation Free Seconds, Transmitter Bipolar Violation Rate, Transmitter Bipolar Violation Seconds, Time of Day, Month/Day/Year, Yellow Alarm Seconds, Greater Than 15 Zeros Seconds
Calculated Results (Interface Module Dependent)	Percent of Error Free Seconds, Percent of One's Density, Percent Frame Bit Error Free Seconds, Percent CRC Error Free Seconds, Power Failures, Wander Positive, Wander Negative, Clock Slip
Special Results	Alarms and Alarm History
G.703-815 Special Results	Transmitter Sync Loss, Transmitter Sync Loss Seconds, Receiver Sync Loss, Receiver Sync Loss Seconds, Transmitter Sync Seconds, Total Elapsed Seconds
Other Measurements	
Delay - Rising or Falling Edge Selectable	Range: 1 usec to 5 minutes, Resolution: ± 1 usec
Start/Stop Signal Sources	RTS, Receive Data, Transmit Data, SQ, DTR, DCD, DSR, and CTS
Network Loop Delay	Range: 1 usec to 5 minutes, Resolution: to ± 1 usec
Frequency	Range and Accuracy - 50Hz to 13MHz @ 1ppm

Table 1-3. Model 5500A Specifications.
(Continued)

CHARACTERISTIC	SPECIFICATION
REAR PANEL CONNECTORS	
USER CLK BNC Connector	
Input Signal Range	50Hz to 13MHz
Logic	1=5+.05 volts DC 0=0+.4 volts DC
Load	10 TTL loads
Outer Conductor	Ground
Inner Conductor	Signal
VIDEO RCA Jack	
Output Signal	RS-170 Composite Video
Signal Level	1 v., p-p
Output Load	50 ohms, minimum
Outer Conductor	Ground
Inner Conductor	Signal
RS-232	
Configuration	DCE/DTE (Switch Selectable)
Type	25-pin, D-Shell
Signal Level	1=-5v to -12v, 0=+5v to +12v
IEEE-488	
Type	IEEE-488 Standard Connector
Signal Level	1=2.5v min, 0=.5v max.
INTERFACE	50-pin Female Connector mates to Male Connector on Model 5500A Interface Modules
REAR PANEL TEST POINTS	
Signal	TXD (Transmit Data), RXD (Receive Data), TXC (Transmit Clock), RC (Receive Clock), XMIT PAT (Transmit Pattern Sync), REC PAT (Receive Pattern Sync), ERR (Bit Error Sync), REC SYNC (5500A in Sync), SP (Spare), GND (Ground)
Signal Level	1=5v+.5v, 0=0v+.4v
Pulse Width	1/2 Bit Time, minimum

Table 1-3. Model 5500A Specifications.
(Continued)

CHARACTERISTIC	SPECIFICATION
REMOTE CONTROL	
Connection	RS-232 Printer/Remote Control Interface and IEEE-488 Bus Interface
Controllable Functions	All Menu Selections, Hexidecimal Keypad Entries, and Front Panel Keys
DISPLAY	
Type and Size	5" High Resolution, monochrome, cathode ray tube
Phosphor	Green
Characters	32 columns x 20 lines, maximum (640 char., max.)
Standard Menus Displayed	BERT, Menu Matrix Help, BERT Format, Bit Trap, Remote Configuration, User Pattern, System Configuration, Graph Display, Print Selection, User Programs, Graph Data Selection, and Big BERT
Optional Menus Displayed	MSU Configuration, High Speed Jitter, and G.821 Parameters
Graph Display	
Data Scale Factors	10^0, 10^1, 10^2, 10^3, 10^4, and 10^5
Time Scale Factors	1 second/division, 10 seconds/division, 1 minute/division, 10 minutes/division, 60 minutes/division
Vertical Scale	0 to 100,000 units
Functions That May Be Graphed	Bit Errors, Errored Seconds, Frame Bit Errors (T1), Frame Bit Errored Seconds (T1), F-Bit Errored Seconds (T1), CRC Errors (T1), Frame Sync Losses (T1), Pattern Sync Losses, Receive BPV Seconds, > 15 Zeros Events (T1), Severely Errored Seconds (T1), Wander + (T1), Wander - (T1)
POWER REQUIREMENTS	
Voltage	User Selectable: 90-130 VAC, or 180-250 VAC
Frequency	45 to 450 Hz
ENVIRONMENTAL	
Temperature	Operating 0° to +50° C; Storage -10° to +85° C
Humidity	90% Non-condensing
Weight	5.25" x 17.20" x 12.79"; weight - 18 lbs.

THIS PAGE LEFT INTENTIONALLY BLANK

5500A Telecommunications Analyzer

Phoenix

Operation – Section 3

Controls/Indicators, Initial Power Up, Menus Frequency Measurement, Event Timing, and Activity Indicators.

34-00057-113TB
1st Edition, 1 Feb 1989
1st Revision, 15 September 1989, Change 1, 1 Jan 90

table of contents

Paragraph		*Page #*
3.0	INTRODUCTION	3-1
3.1	CONTROLS AND INDICATORS	3-1
3.2	INITIAL POWER UP	3-12
3.3	MENUS	3-13
3.3.1	Help Menu	3-13
3.3.2	5500A Configuration Menu	3-14
3.3.3	BERT Setup Menu	3-17
3.3.3.1	RS-232 BERT Setup Menu	3-18
3.3.3.2	T1 ESF BERT Setup Menu	3-22
3.3.4	BERT Results/Parameters Menu	3-30
3.3.4.1	RS-232 BERT Results/Parameters Menu	3-30
3.3.4.2	ESF T1 BERT Results Menu	3-33
3.3.5	Printer Setup Menu	3-33
3.3.6	Graph Setup Menu	3-36
3.3.7	Graph Display	3-38

Table of Contents (Continued)

Paragraph		*Page #*
3.3.8	RS 232/IEEE488 Menu	3-41
3.3.9	Store/Recall Setups Menu	3-42
3.3.10	User Pattern Menu	3-44
3.3.11	BIG BERT Display	3-45
3.3.12	Digital Data Trap Menu	3-48
3.3.13	Other Menus	3-52
3.4	FREQUENCY MEASUREMENT	3-52
3.5	TIME MEASUREMENTS	3-53
3.5.1	Event Timing	3-53
3.5.2	Network Loop Timing	3-53
3.6	BIAS DISTORTION (SKEW)	3-54
3.7	BER TEST ASSISTANCE	3-54
3.8	ACTIVITY INDICATORS	3-54

List of Figures

Title	*Figure #*	*Page #*
Model 5500A Front Panel Controls and Indicators	Figure 3-1	3-6
Model 5500A Rear Panel Controls and Indicators	Figure 3-2	3-11
RS-232 BERT Setup Menu	Figure 3-3	3-12
5500A Configuration Display	Figure 3-4	3-13
Help Menu Display	Figure 3-5	3-14
5500A Configuration Menu	Figure 3-6	3-15
Systems Options Setup Menu	Figure 3-7	3-16
RS-232 BERT Setup Menu	Figure 3-8	3-19
ESF T1 BERT Setup Menu	Figure 3-9	3-23
RS-232 BERT Results/Parameters Menu	Figure 3-10	3-31
T1 ESF BERT Results Menu	Figure 3-11	3-34
RS-232 Printer Setup Menu	Figure 3-12	3-35
ESF T1 Printer Setup Menu	Figure 3-13	3-36
Graph Setup Menu	Figure 3-14	3-37

List of Figures (Continued)

Title	*Figure #*	*Page #*
Graph Display	Figure 3–15	3–39
RS 232/IEEE488 Menu	Figure 3–16	3–42
Store/Recall Setups Menu	Figure 3–17	3–43
User Pattern Menu	Figure 3–18	3–44
Big BERT Display	Figure 3–19	3–48
Digital Data Trap Display	Figure 3–20	3–49
Digital Data Trap Display After User Softkey is Pressed	Figure 3–21	3–50
5500A Network Loop Delay	Figure 3–22	3–53

List of Tables

Table #	*Title*	*Page #*
Table 3–1.	Model 5500A Front Panel Controls and Indicators.	3–1
Table 3–2.	Model 5500A Rear Panel Controls and Indicators.	3–7
Table 3–3.	Error Injection Modes.	3–25
Table 3–4.	Clock Source Selections for ESF T1	3–27
Table 3–5.	Graph Definitions.	3–40
Table 3–6.	Hex to Binary Conversion.	3–46
Table 3–7.	BER Test Assistance	3–55
Table 3–8.	RS–232/RS–449 Activity Indicators.	3–57
Table 3–9.	T1/T1C and V.35 Activity Indicators.	3–58

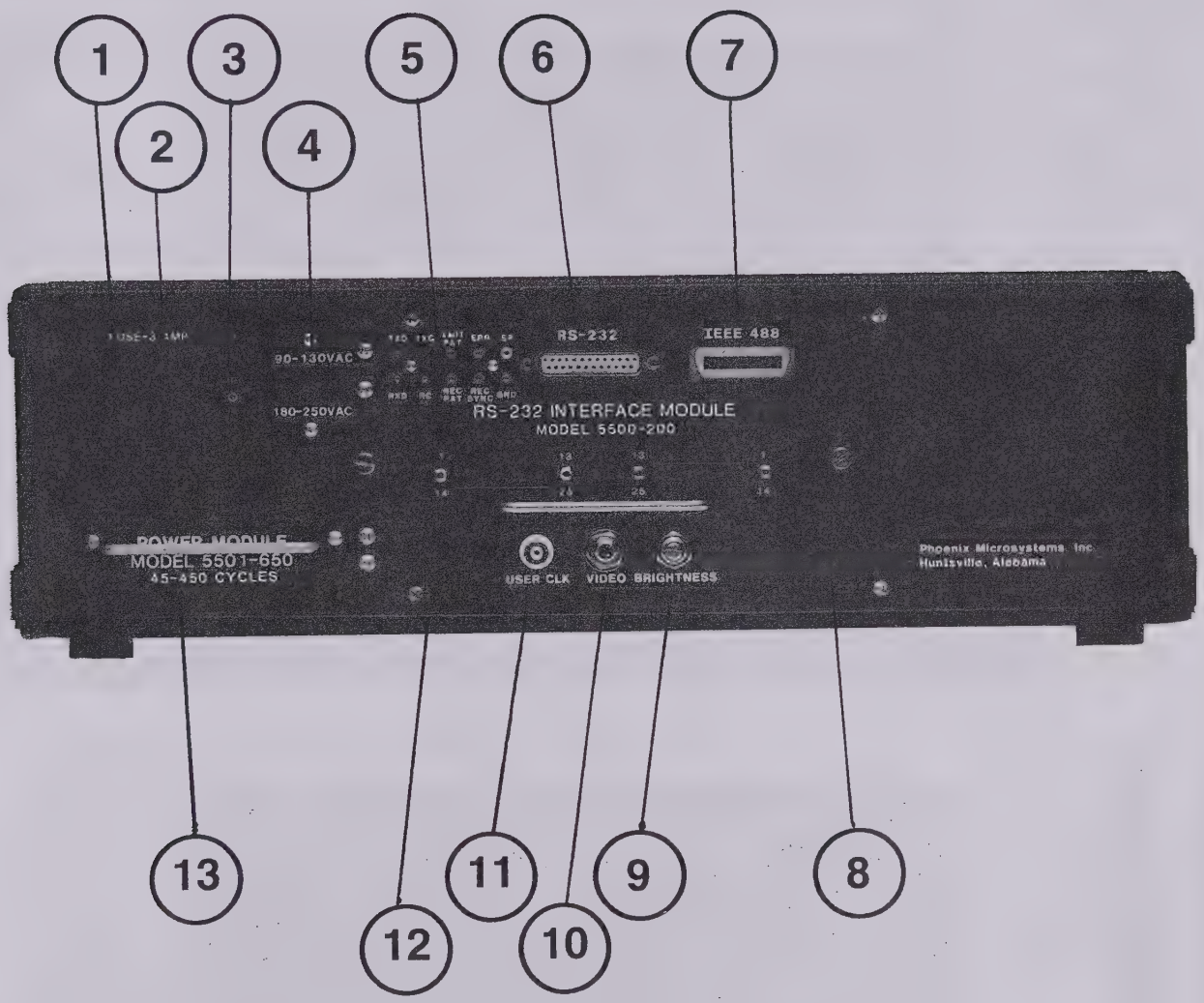
List of Effective Pages

* 0 in this column indicates original page

Page No	*Change No	Page No	*Change No	Page No	*Change No
3-1 to 3-11	0				
3-12 to 3-58	1				

RECORD OF CHANGES

CHANGE NUMBER	CHANGE DATE	CHANGE NUMBER	CHANGE DATE	CHANGE NUMBER	CHANGE DATE
Preliminary	11/88				
1st Edition	2/89				
1st Revision	9/89				
Change 1	1/90				



Model 5500A Rear Panel Controls and Indicators
Figure 3–2

3.2 INITIAL POWER UP

The following steps are provided for the first time user of the Model 5500A. It provides information required to turn the Model 5500A on, select the desired menus, and how to make changes on the menus. Specific instructions for each menu follow this section.

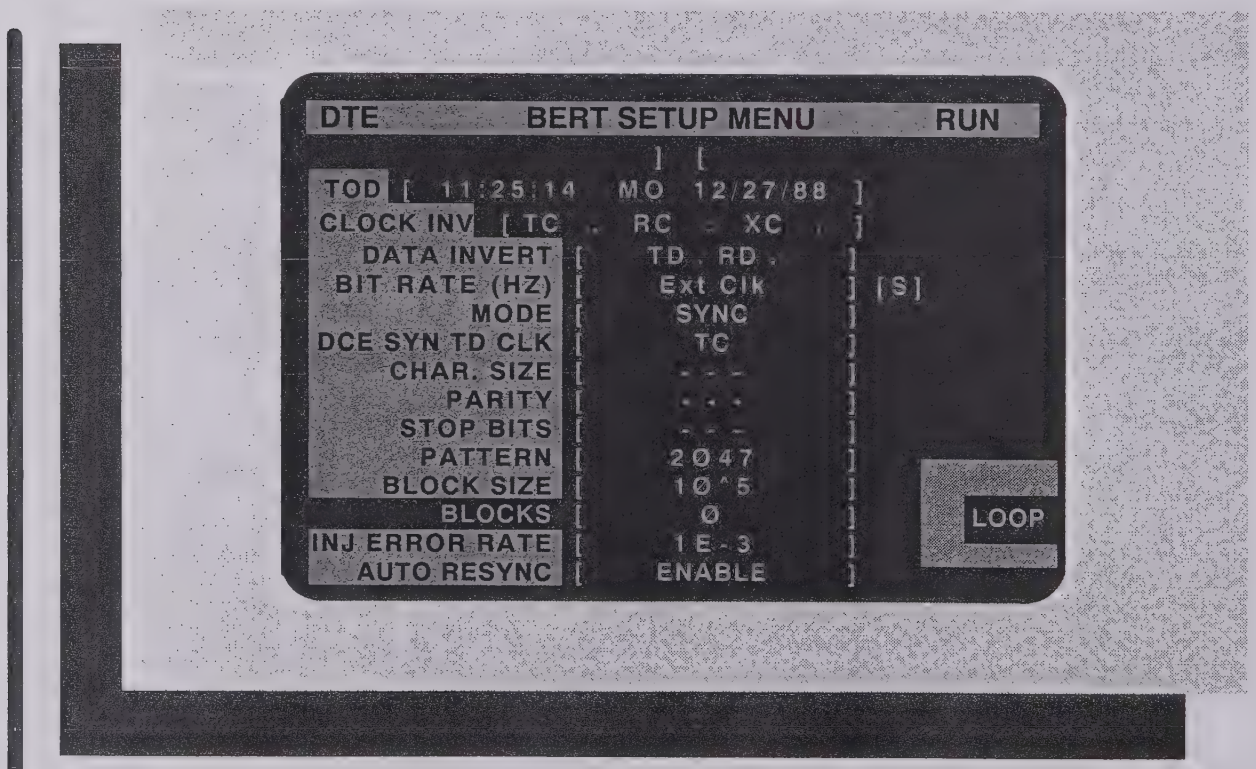
1. With power removed, plug the desired interface module into the rear panel slot on the Model 5500A and secure with the two retaining screws.

2. Check the power select switch (refer to Figure 3-2) to ensure the Model 5500A voltage is set to match the local source voltage.

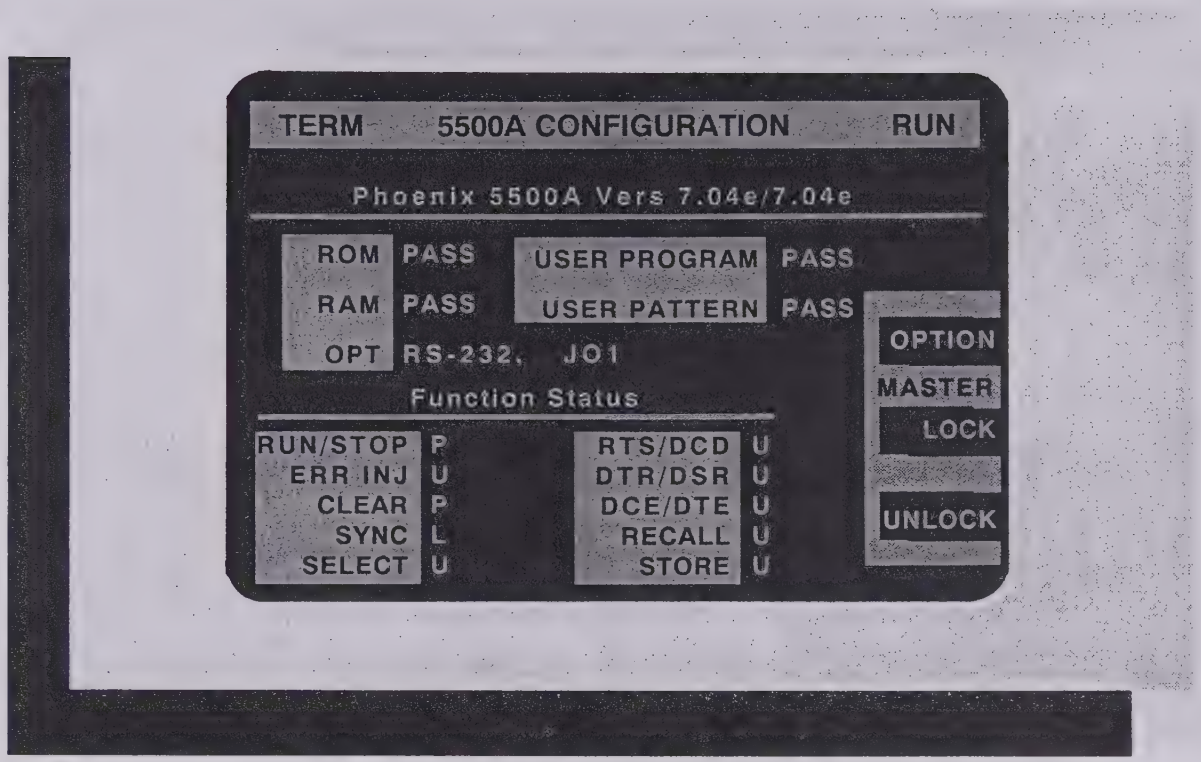
3. Turn the power switch (refer to Figure 3-2) to on.

4. The first item to appear will be either the BERT setup screen (Figure 3-3) or the 5500A Configuration display (Figure 3-4).

5. If the display is the 5500A Configuration display (Figure 3-4), it means that the 5500A has failed the self-test or that the USER PROGRAM or USER PATTERN has an error or has not been programmed. If the display indicates a ROM or RAM failure, return to step one and begin this procedure again. If the problem persists, return the unit to Phoenix microsystems, inc. for repair. If the USER PROGRAM or USER PATTERN indicate invalid, you may proceed with testing; however, the program/pattern stored in memory is suspect. This may be due to battery failure. In


DTE
BERT SETUP MENU
RUN
TOD [11:25:14 MO 12/27/88]
CLOCK INV [TC , RC , XC ,]
DATA INVERT [TD , RD ,]
BIT RATE (HZ) [Ext Clk] [S]
MODE [SYNC]
DCE SYN TD CLK [TC]
CHAR. SIZE [- - -]
PARITY [- - -]
STOP BITS [- - -]
PATTERN [2047]
BLOCK SIZE [10^5]
BLOCKS [0]
INJ ERROR RATE [1E-3]
AUTO RESYNC [ENABLE]
LOOP

RS-232 BERT Setup Menu
Figure 3-3



5500A Configuration Display
Figure 3-4

any case, do not use the stored pattern/program until it has been verified.

The Model 5500A is now ready to be used for setup and testing. The following paragraphs will detail the various menus and how they are setup and testing.

3.3 MENUS

The 5500A uses a series of menus, or displays, to provide the user with information and allow the flexibility which is needed in todays test equipment.

The 5500A uses 14 standard menus which are arranged in a matrix as illustrated on the 5500A front panel. Menus are provided to ease operation where large numbers of test functions or results make conventional analog or metered displays impractical.

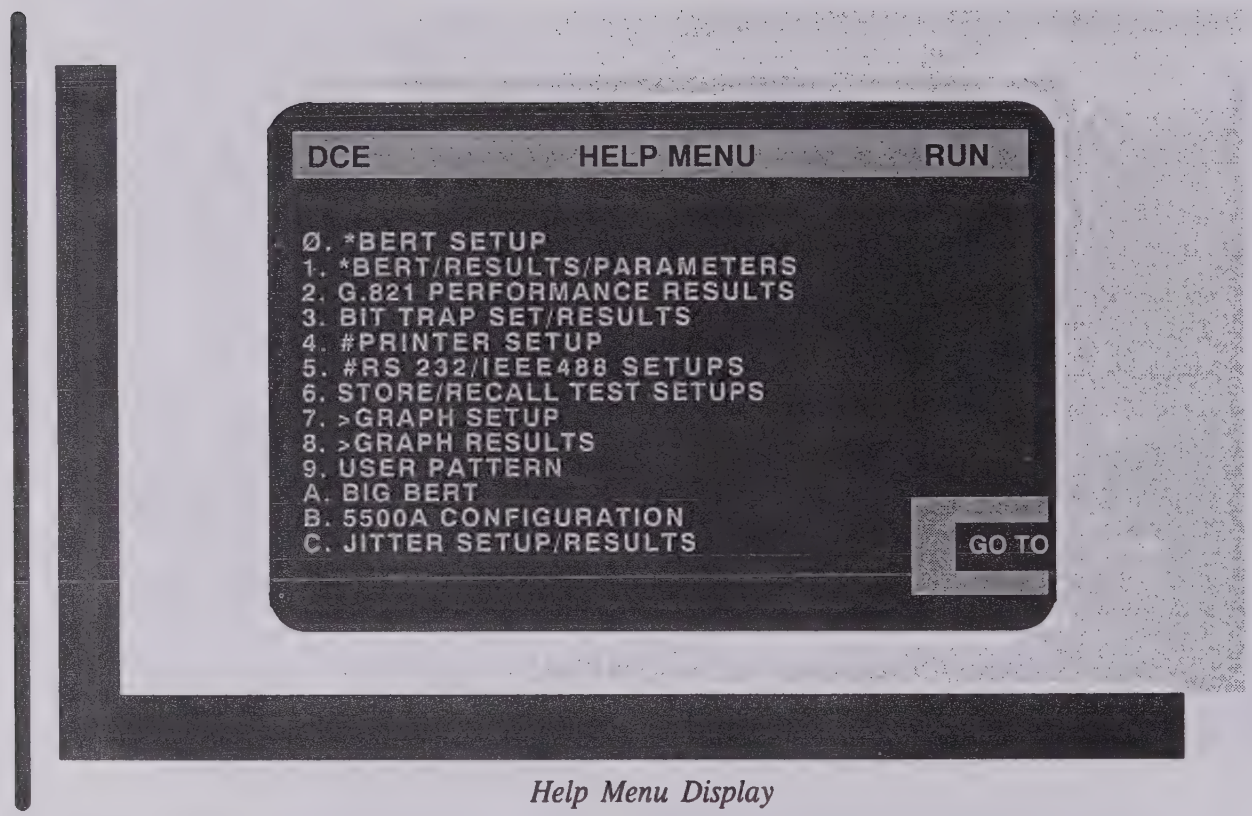
In this section of the manual we will examine all the standard menus for the RS-232 module and the differences in those menus when the Model 5500A-628 ESF T1 module is inserted into the 5500A.

3.3.1 Help Menu

The help menu, Figure 3-5, provides the user with a listing of all the menus. This menu remains essentially the same for all interface options. To use this menu, follow the steps below:

1. Press the RECALL key one time to bring the menu matrix help display to the screen.

2. The softkey for this menu is labeled GO TO on the menu and is the bottom key of the three softkeys on the front panel (refer to Figure 3-1). Pressing this softkey brings



Help Menu Display
Figure 3-5

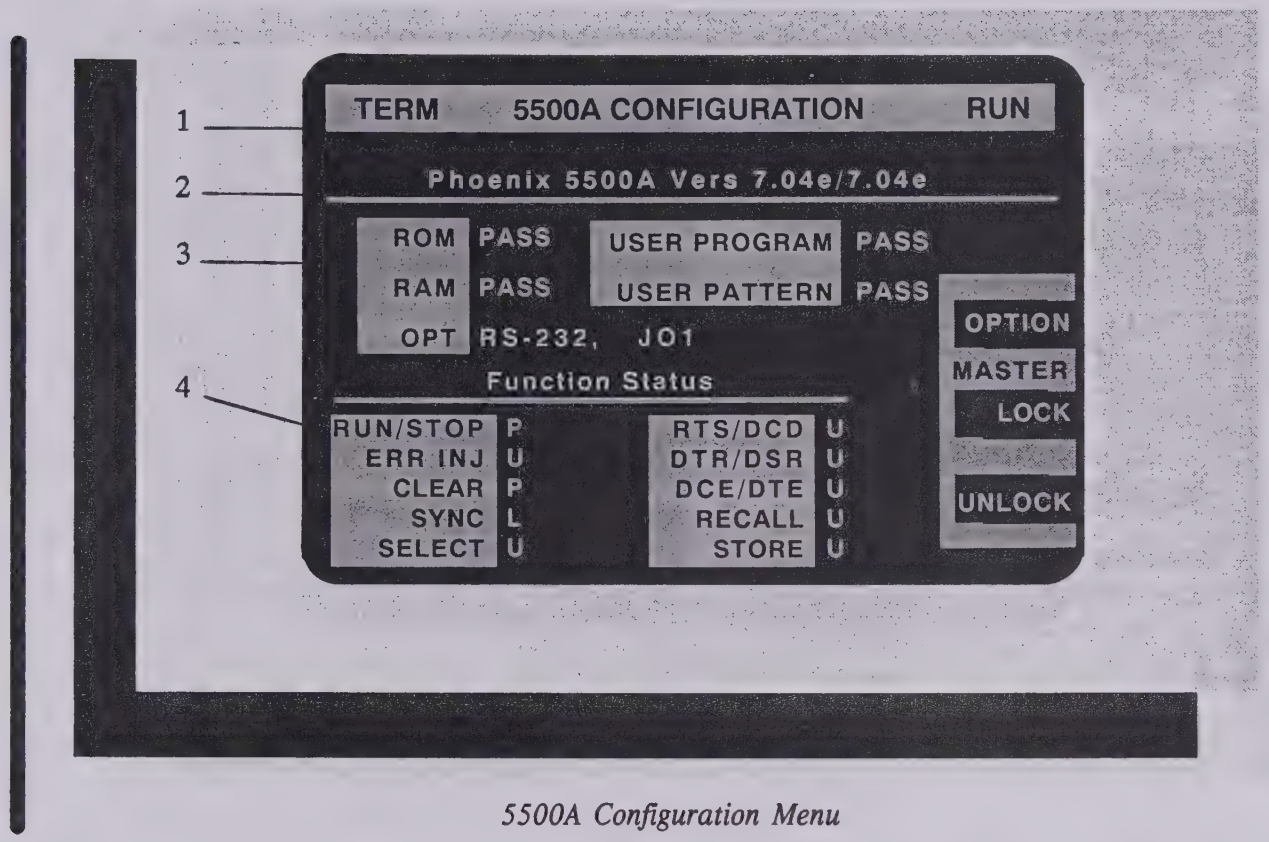
to the screen the menu selected by the cursor. In Figure 3-5, the cursor is shown over menu # 8, User Pattern. If the softkey were pressed in this example, the help menu would be replaced by the User Pattern menu. Menus that are preceeded with an identifer (*BERT Setup and *BERT Results/Parameters, #Printer Setup and #RS232/IEEE488 Setups, and >Graph Setup and >Graph Results) are used are used in conjunction with each other.

3. The cursor can be moved on this menu by pressing a number or letter on the keypad will move the cursor directly to that number in the matrix and the corresponding number on the list of menus.

3.3.2 5500A Configuration Menu

The 5500A Configuration Menu, presented in Figure 3-6 is used to view overall 5500A system operation and provide a method to lock various controls.

The softkeys for this menu are the master lock and options menu select. When the LOCK softkey is pressed, all the front panel controls listed on this menu are disabled. When the UNLOCK softkey is pressed, it unlocks all the function keys on this menu that had been locked. It is always a good idea to press the UNLOCK softkey prior to setting up the 5500A to run any test. Failure to notice that one of the front panel keys has been locked out can cause the user to spend many needless hours



5500A Configuration Menu
Figure 3-6

agonizing over how to get the 5500A to perform a particular function.

When the OPTION softkey is pressed, the SYSTEM OPTIONS SETUP menu, illustrated in Figure 3-7, is brought to the screen. This menu is used to establish operating parameters for the 5500A as follows:

CRT REFRESH

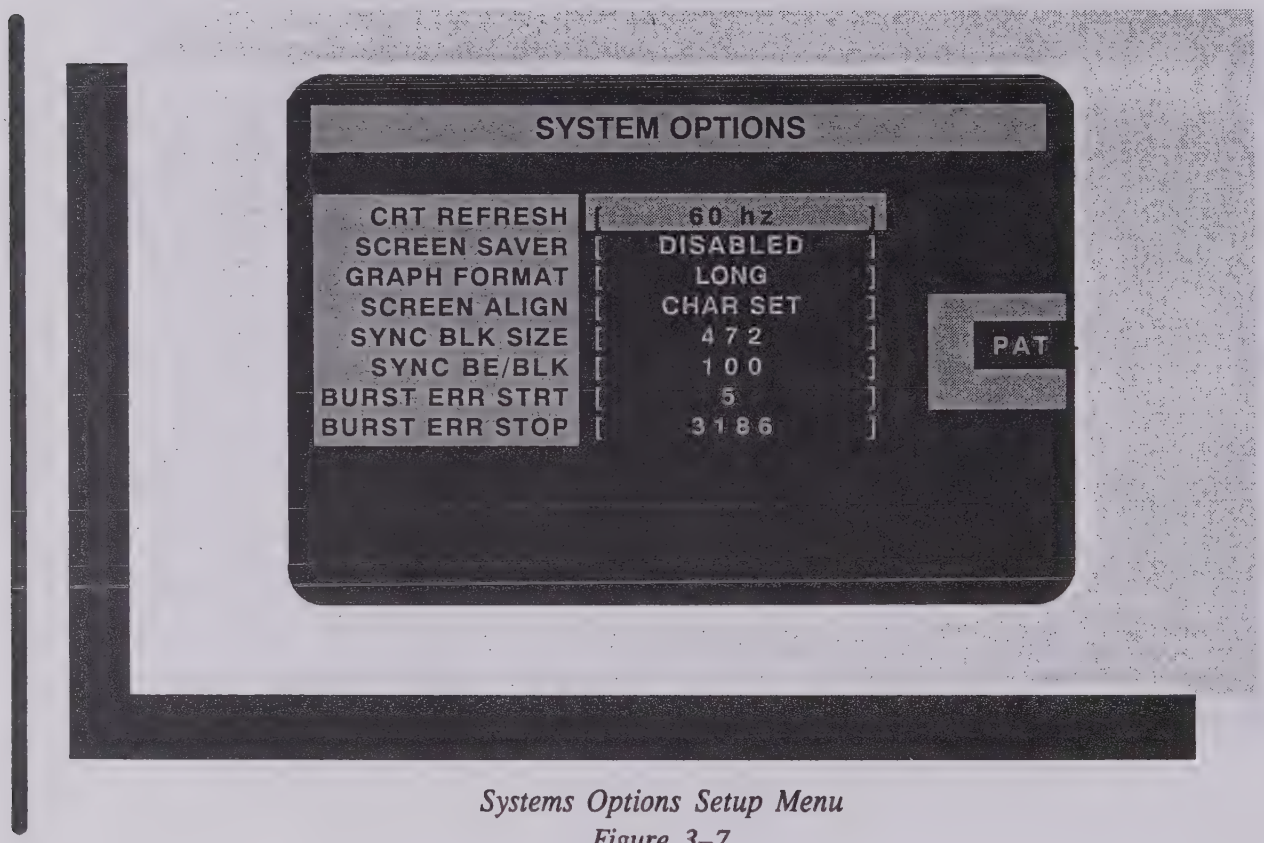
The 5500A CRT is refreshed at a frequency that is a multiple of the line frequency. The user must set the line frequency using this line of the display. Use the **CURSOR** keys to place the cursor over the CRT REFRESH field and use the **SELECT** keys to select 50 hz or 60 hz.

SCREEN SAVER

The screen saver option turns off the CRT display approximately 10 minutes after the last key was pressed on the 5500A. Pressing any key on the 5500A will turn the display back on for another 10 minutes. This option is DISABLED or ENABLED by moving the cursor over the SCREEN SAVER field and using the the **SELECT** keys to select DISABLED or ENABLED.

GRAPH FORMAT

There are two ways the graph may be printed out on a printer. The LONG presentation is most frequently used and prints the entire graph data in a bar graph format. The SHORT presentation prints all the numeric data but does not print the bars on the graph. This option is most often used to conserve bits when the graph data is being sent to a remote site via a modem. Selection of LONG or SHORT is made with the **CURSOR** and **SELECT**


SYSTEM OPTIONS
CRT REFRESH [60 hz]
SCREEN SAVER [DISABLED]
GRAPH FORMAT [LONG]
SCREEN ALIGN [CHAR SET]
SYNC BLK SIZE [472]
SYNC BE/BLK [100]
BURST ERR STRT [5]
BURST ERR STOP [3186]
PAT

Systems Options Setup Menu
Figure 3-7

keys in the same manner as the previous selections.

SCREEN ALIGN

This option is used to select CHAR SET or ALIGN #1 screens to be used to align the display on the face of the CRT during final pre-shipment testing of the 5500A. The alignment can be performed in the field if required by following the procedure below:

1. Select either of the alignment screens (CHAR SET or ALIGN #1). There is no difference in the alignment procedure between the alignment screens. Selection of the particular screen is a matter of user preference.

2. Press the **PAT** softkey. (The display will change to the selected screen alignment pattern.)

3. Use the **CURSOR** keys to move the display on the screen to the desired location.

4. Press a **SELECT** key to return to the SYSTEM OPTIONS SETUP menu.

SYNC BLK SIZE
SYNC BE/BLK

These two lines are used to establish the threshold for sync loss. The block size may be set to any value between 1 and 100,000 and the bit errors per block may be set to any value between 1 and 50,000. The factory setting of these values are a block size of 1000 with a bit errors per block of 100 or an error rate threshold of 1E-01.

To set a value to either line, place the cursor over the desired field and use the front panel hex keypad to enter the desired value.

NOTE

The values selected for block size and bit errors per block remain stored in memory and will **NOT** default to the factory setting on power up.

BURST ERR STRT
BURST ERR STOP

The 5500A has incorporated a burst error detection circuit to aid the user in determining the distribution of errors. Burst errors (BURS on the ESF T1 BERT menu) are considered a group of errors so closely grouped that for all intents and purposes, they are "one event".

These two lines of the system options display are used to set the starting and ending error thresholds that define a "burst". The burst error start may be programmed from 1 to 15 consecutive errors while the burst error stop may be programmed from 1 to 50,000 consecutive error free bits.

This feature is particularly useful when a long term, unattended test is being run. Assume that the burst error start has been set to 1 consecutive bit errors and that 1000 consecutive error free bits has been selected as the burst error stop threshold. After a 24 hour period, the 5500A indicates that 74 bit errors took place, but only one burst error took place. The user then knows that all the bit errors took place in one "burst" and except for that period of time, the circuit under test was error free.

The following paragraphs explain the remaining lines presented on the 5500A Configuration Menu. Refer to Figure 3-6:

1. This line is the same as the top line on the BERT Setup and BERT Results/Parameter menus. This line will change with the various interface menus. It will reflect DCE/DTE or the termination status of the module (LOOP, BRDG, TERM).

2. This line will present the software revision of the Model 5500A. The display shown has software version 7.04e installed.

3. This area of the display is used to present the results to the Model 5500A power up self-test. The ROM, RAM, USER PROGRAM, and USER PATTERN are checked. The OPT line lists the various interface options and/or jitter options that are installed.

4. This area of the display allows the user to set the status of the front panel controls on the 5500A. By placing the cursor over the letter to the right of the control name, pressing the cursor select keys will scroll the letter from P to U to L. The L indicates the control is locked and pressing that key will have no effect. The U indicates the key is unlocked and pressing it will cause it to function in its normal manner. P is the protected status and prevents that key from being accessed from the remote terminal.

3.3.3 BERT Setup Menu

The BERT Setup menu, located at position 0 on the help menu, is one of the most important menus in the operation of the 5500A as it is used to setup the majority of the test conditions. The menu is brought to the display by the following steps:

1. Perform the power up procedure in section 3.3 above.

2. Press the HELP-1 key one time to bring the menu matrix help screen to the display.

3. Press the 0 key on the keypad.

4. Press the GO TO softkey.

The BERT SETUP menu, Figure 3-8 or Figure 3-9, should now be present on the screen.

3.3.3.1 RS-232 BERT Setup Menu

The RS-232 BERT Setup menu is illustrated in Figure 3-8. The key line numbers correspond to the numbers below that explain each line of the menu. The softkey for this menu is the LOOP key which places the 5500A in the self-test loopback mode. Changes are made on this menu by moving the cursor over the desired parameter and then using the cursor SELECT keys to scroll the desired value under the cursor.

The lines on the BERT setup menu are as follows:

1. DTE/DCE - This section of the top line indicates what the 5500A is emulating, DTE or DCE.

2. TOD - This line contains the time of day and day/date/year. The correct time/date is set on this menu and once set, the information is retained in memory.

3. CLOCK INV - The user may elect to invert the polarity of the transmit (TC), receive (RC) or external (XC) clock signals. A dot (.) following the clock indicates the clock is NOT inverted. To invert the clock, place the cursor over the dot and press the CURSOR SELECT key. The dot will be replaced with an 'I' indicating that clock has been inverted.

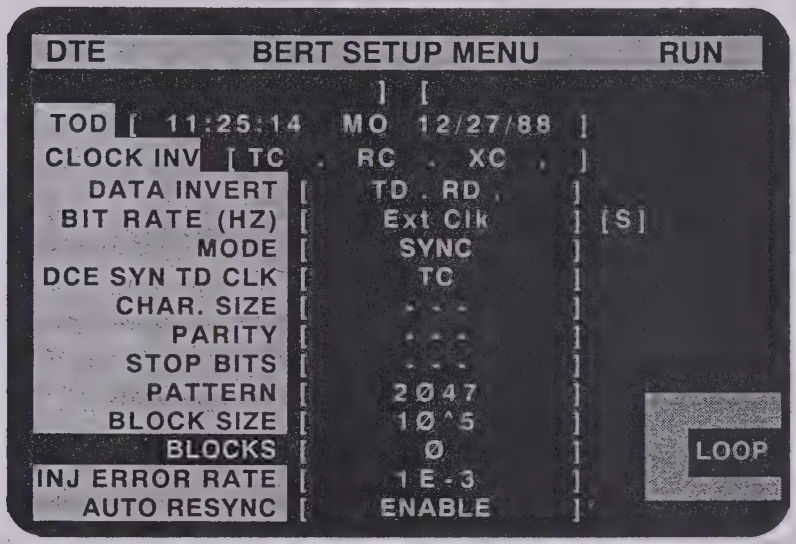
4. DATA INVERT - This line works in the same manner on the receive data (RD) and transmit data (TD) as the clock invert above.

5. BIT RATE - The internal bit rates which can be selected are listed in Figure 3-8. The [O or S] field choice to the left of the bit rate field refers to the optional specific frequency which the user may choose to enter. The synthesizer permits the user to select any data rate by entering the frequency through the use of the HEX keypad. By selecting the [S] field, the user may select any of the standard bit rates. The USER CLK choice refers to the rear panel clock input on the Model 5500A. The user may input a frequency synthesizer to the USER CLK BNC connector and select any frequency from 75 bps to 13 bps for operation.

The HEX keypad is used to enter the bit rate and edit the bit rate field. The "0 - 9" keys are used to enter the numbers into the bit rate field. After the desired bit rate is entered, the "E" key is used to enter the bit rate selected. The "C" key serves as a CLEAR or DELETE key and will delete the last entry made. This key may be used in either the 'edit' or 'select' mode. The "D" key serves as the decimal point in those bit rates between 50.0 and 499999.9. For selections greater then 499999.9, the D key is not valid and the 5500 will respond with a 'BEEP' if the D key is used outside it's range.

6. MODE - The Model 5500A is capable of synchronous or asynchronous operation. Generally speaking, most systems operating at 2400 baud and above are synchronous with the exception of certain compressed bit rate voice systems. The

PATTERNS AVAILABLE ON LINE 11
63, 511, 2047, REV 2047, (2^15)-1, (2^20)-1, QRW, T1 SET, T1 RESET, MARK, SPACE, ALT, FOX, SYSY 511, X25 511, NET55, USR1, USR2, USR3, USR4.


DTE
BERT SETUP MENU
RUN
TOD [11:25:14 MO 12/27/88]
CLOCK INV [TC . RC . XC .]
DATA INVERT [TD . RD .]
BIT RATE (HZ) [Ext Clk] [S]
MODE [SYNC]
DCE SYN TD CLK [TC]
CHAR. SIZE [- - -]
PARITY [- - -]
STOP BITS [- - -]
PATTERN [2047]
BLOCK SIZE [10^5]
BLOCKS [0]
INJ ERROR RATE [1E-3]
AUTO RESYNC [ENABLE]
LOOP

BIT RATES THAT MAY BE SELECTED ON LINE 5

(Must be in standard (S) mode - optional mode (O) permits selection of any rate between 50 Hz and 13 Mhz.)

BPS			KBPS			MBPS
75	110	134.5	14.4	16	19.2	1.024
150	200	300	24	28.8	32	1.344
600	1200	1800	48	56	57.6	1.544
2400	3200	3600	64	72	76.8	
4800	6400	7200	84	96	112	
8000	9600		115.2	128	144	**OTHER**
			153.6	168	192	
			224	230.4	256	Opt Clk
			288	336	384	Ext Clk
			448	460.8	512	User Clk
			576	672	768	

RS-232 BERT Setup Menu
Figure 3-8

Model 5500A can operate at bit rates up to 48 Kbps asynchronously.

In asynchronous operation, all transmitted data is characterized by the inclusion of a specific number of data bits, stop bits, and parity check. The user must select these items and they are described in steps 8, 9, and 10 that follow.

7. DCE SYN TD CLK – (DCE mode synchronous transmit data clock) When the user selects DCE simulation operation of the Model 5500A it is necessary to then select whether the test set (simulating a MODEM) will supply clock (TC–Pin 15) to, or derive clock (XC–Pin 24) from the system under test in synchronous operation. If the user selects TC then the Model 5500A transmitter's clock source is its own internal clock. If XC is chosen then the Model 5500A transmitter derives its timing from the system under test. Note that this selection is only meaningful in synchronous DCE mode simulation and is primarily used only when operating at speeds greater than 1 Mhz.

8. CHAR SIZE – The number of data bits which make up a character in asynchronous data transmission is selectable from either the FORMAT or main BERT menus. Asynchronous character sizes of 5, 6, 7, or 8 bits length may be chosen. If CONTINUOUS is chosen then the Model 5500A sends out a continuous stream of data bits without start and stop characters. When operating in a synchronous mode there are no start and stop bits and so the bit stream is continuous or infinite and three dashes are displayed in the menu field.

9. PARITY – Parity bits in the data stream provide a means of error detection. In async data streams the user may select EVEN or ODD parity or may choose NO parity at all. Choosing EVEN parity means that the number of 1's in a data block must add up to an even number. Likewise ODD parity means the number of 1's in the block of data sums up to an odd number. If, in EVEN parity, a block is received with three 1's in it, then the detector knows there has been at least one error. The choice of parity or no parity depends entirely on the system under test. The parity bits are not used in synchronous data streams, therefore three dashes appear in parity field when the synchronous mode has been selected.

10. STOP BITS – Asynchronous, Byte oriented data transmissions employ start and stop bits to identify one byte from the next. A typical data transmission may be composed of a start bit, seven data bits, a parity bit and a stop bit. The choice of STOP BITS is either 1 or 2 and depends upon the system under test. This parameter has no meaning in synchronous transmission, and therefore the field contains three dashes.

11. PATTERN – The choice of pattern depends upon the test which the user desires to make. The Model 5500A uses industry standard pseudorandom sequences of various lengths for Bit Error Rate testing (refer to Figure 3–8) plus a number of other patterns for specific uses as well as a USER programmable pattern up to 135 HEX characters long.

A NET55 pattern is included for those users that have been using the 2^{15}–1 as an alternative to the QRW pattern to stress test network spans. Unfortunately, the 2^{15}–1

pattern violates the 1's density specification in publication 62411 thus giving span vendors the option of ignoring the test results.

The NET55 stress pattern meets all the specifications in publication 62411. It has also been proven in field trials as being able to cause marginal spans to fail more consistently than the 2^{15}–1 or QRW patterns. Phoenix suggests that this pattern be run with the frame disabled in the T1 setup.

A FOX–2 pattern is available for testing low speed applications. When used in the async mode the character size selection also sets the coding format as follows:

Character Size	Code Format
5	BAUDOT
6	EBCDIC
7	ASCII
8	BCDIC

In the synchronous mode the FOX–2 pattern is coded as 8–bit ASCII.

12. BLOCK SIZE – The number of bits which make up a block can be selected as follows:

10^2 100 bits/block
10^3 1,000 bits/block
10^4 10,000 bits/block
10^5 100,000 bits/block
10^6 1,000,000 bits/block
10^7 10,000,000 bits/block
10^8 100,000,000 bits/block
10^9 1,000,000,000 bits/block

The choice of block size is a factor in the overall test length in bits since the block size times the number of blocks in the test equals a specific number of bits. The choice of block size may be dictated by any number of factors, such as the simulation of the actual signals, but in general the higher the bit rate, the larger the block size.

13. This line may be set to BLOCKS or TEST TIME by placing the cursor over BLOCKS or TEST TIME and using the **SELECT** keys to toggle between the two choices.

When BLOCKS has been selected the number of blocks in the test may be selected as any number from 1 to 9999. If a "0" is placed in this window, then the Model 5500A will run a test continuously until the **STOP** key is pressed. If a number is entered in the BLOCKS field, the test will stop when the number of blocks tested is equal to the number entered in the BLOCKS field.

The user selects the BLOCKS by moving the half intensity marker to the field to the right of BLOCKS and setting in the desired number using the HEX keypad numbers.

When TEST TIME has been selected in this field, the length of time that the test is to be run is entered in the field to the right of TEST TIME. In the example shown in Figure 3–8, a test length of 4 hours 35 minutes and 16 seconds has been entered through the use of the front panel keypad. The 5500A will stop the test after the selected time increment has elapsed. Entering 00:00:00 will result in a continous running test.

NOTE

The 5500A sends an automatic "Service Request" on the IEEE488 bus at the end of the test.

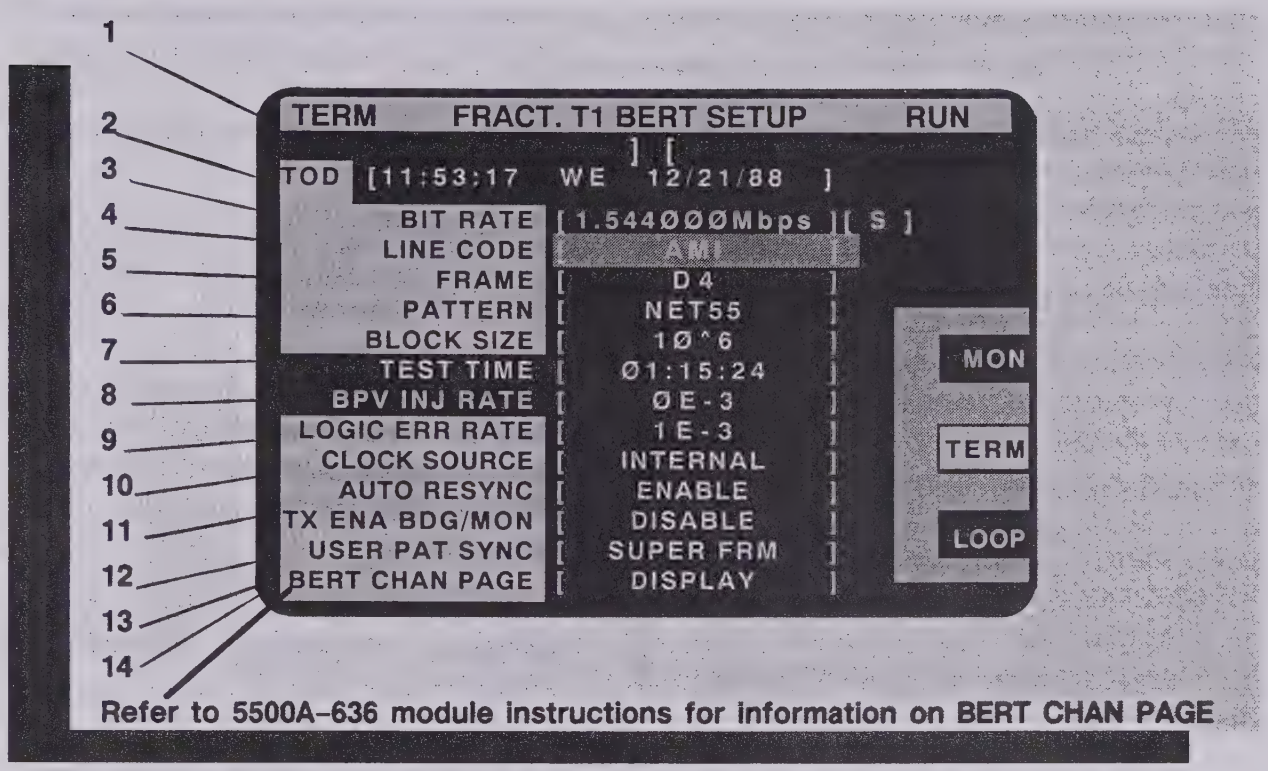
14. INJ ERROR RATE - The Model 5500A enables the user to inject single or multiple bit errors at rates from 5E-2 to 1E-9 errors/bit. The user programs the error rate by scrolling the half intensity block over the INJ ERROR RATE field. The user must select the mantissa of the rate desired using either the SELECT keys or the HEX keypad. The choices are 0 to 9. A "0" (zero) will disable the error inject. Then the user must use the CURSOR key to move the block to the right and change the exponent from -2 to -9 as desired. Once set, the rate is retained in non-volatile memory. Error injection is most often used for identification and testing the integrity of a circuit.

16. AUTO RESYNC - The auto resync function in the model 5500A has three states; enable, disable, and timed. When the auto resync feature is disabled, the 5500A will continue to count bit errors once synchronization has been obtained, regardless of the number of bit errors per unit time. When the auto resync is enabled, the 5500A obtains synchronization and then continually monitors the bit error count and, when the bit error rate exceeds a predetermined threshold, the 5500A will declare it has lost synchronization and will not recover synchronization until a preset number of bits matches the pattern, usually set at 56 bits. During this time the 5500A is out of synchronization, error parameter collection is suspended, with only the time the unit is out of synchronization being accumulated.

In the timed resync mode, a number of 10 millisecond intervals (0-999, representing 0 to 9.99 seconds) is selected by the user as the time span of an internal timer. During the time cycle, if at least one bit error occurs during each 10 millisecond interval, the 5500A will count these errors until the timer runs out. When the timer runs out, the 5500A will check the bit error sync threshold to determine if sync should be broken. If the 5500A breaks sync, it will enter the auto resync disable mode and restart the internal timer. During the timer period, two events are taking place; 1) the 5500A is continuing to accumulate bit errors and, 2) the 5500A is monitoring the data to determine if errors have ceased. If only one 10 millisecond interval is error free, the timer is reset. If errors have ceased, the 5500A continues and the timer is reset, awaiting the next bit error occurrence.

3.3.3.2 T1 ESF BERT Setup Menu

The T1 ESF BERT Setup menu is illustrated in Figure 3-9. The key line numbers correspond to the numbers below that explain each line of the menu. There are three softkeys for this menu. The bottom softkey is the **LOOP** key which places the 5500A in the self-test loopback mode. The top two softkeys are used to select the appropriate termination mode; Bridge, Terminate, or Monitor using the following guidelines:



ESF T1 BERT Setup Menu
Figure 3–9

NOTE

The top soft key is the **MON** key. Activate this key to the "highlighted" state for "MONITOR" mode. Deactivate the **MON** key to the "not highlighted" state to return to the highlighted BRDG or TERM mode. The middle softkey is an alternate function **TERM/BRDG** key. Activate this softkey to change from the displayed mode (i.e. TERM) to the alternate mode (i.e. BRDG).

BRDG mode (BRIDGE high impedance termination option; SAFEST for the curious when wishing to avoid interference with the monitored circuit).

TERM mode (terminates the RX pair with 100 ohms — to be used only when the monitored circuit "terminates" at the Model 628 test interface — normally used only in out–of–service testing when the test set is substituted for the normal network terminating device).

MON mode (MONITOR mode is specifically for DSX panel test access via a standard DSX "MONITOR" jack which provides two 430 ohm resistors in series with tip and ring — in this mode the test set will terminate the RX pair with 100 ohms, resulting in 20dB attenuation of the resistor isolated monitor signal. The resistors minimize circuit interference which might otherwise result from the test set load impedance, test probe contact bounce transients, or an improper test connection to a transmitter instead of a receiver.) The MONITOR mode invokes a 20dB amplifier (voltage gain of 10) to compensate for the 20dB attenuation of the 430 ohm resistors. The BRIDGE mode of termination is compatible with resistor

isolated MONITOR jacks (by virtue of high impedance termination and 628 receiver amplitude tolerance); however, the MONITOR mode is more appropriate when remote test access requires test lead length in excess of fifteen feet. MONITOR jack remote test access wire lengths in excess of 2000 feet may be accommodated by using standard, Z0 = 100 ohm, wiring -- with the 628 module in the MONITOR mode.

Changes are made on this menu by moving the cursor over the desired parameter and then using the cursor SELECT keys to scroll the desired value under the cursor.

The following is a description of the lines on the T1 BERT setup menu:

1. This line gives the status of the termination mode selected (TERM, BRDG, MON) with the softkeys as described above.

2. TOD – This line contains the time of day and day/date/year. The correct time/date is set on this menu and once set, the information is retained in memory.

3. BIT RATE (HZ) – This line shows the bit rate for the interface module (in this case T1). There are two fields associated with this line. The [O] or [S] field to the left of the bit rate line permits the user to select "S" for the standard bit rate for the module (in this case, 1544000). By selecting "O", the operator may choose any bit rate desired through the use of the front panel keypad.

4. LINE CODE – This line is used to select the desired line code, AMI (alternate mark inversion) or B8ZS (bit eight zero suppression).

5. FRAME – This line is used to select the framing format desired. Choices are SLC-®96, ESF, D4, or DISABLE. The DISABLE selection would be made if it was desired to test unframed data at the T1 data rate.

6. PATTERN – The choice of pattern depends upon the test which the user desires to make. The Model 5500A uses industry standard pseudorandom sequences of various lengths for Bit Error Rate testing (refer to Figure 3–8) plus a number of other patterns for specific uses as well as a USER programmable pattern up to 135 HEX characters long.

7. BLOCK SIZE – The number of bits which make up a block can be selected as follows:

10^2	100 bits/block
10^3	1,000 bits/block
10^4	10,000 bits/block
10^5	100,000 bits/block
10^6	1,000,000 bits/block
10^7	10,000,000 bits/block
10^8	100,000,000 bits/block
10^9	1,000,000,000 bits/block

The choice of block size is a factor in the overall test length in bits since the block size times the number of blocks in the test equals a specific number of bits. The choice of block size may be dictated by any number of factors, such as the simulation of the actual signals, but in general the higher the bit rate, the larger the block size.

8. This line may be set to BLOCKS or TEST TIME by placing the cursor over BLOCKS or TEST TIME and using the **SELECT** keys to toggle between the two choices.

When BLOCKS has been selected the number of blocks in the test may be selected as any number from 1 to 9999. If a "0" is placed in this window, then the Model 5500A will run a test continuously until the **STOP** key is pressed. If a number is entered in the BLOCKS field, the test will stop when the number of blocks tested is equal to the number entered in the BLOCKS field.

The user selects the BLOCKS by moving the half intensity marker to the field to the right of BLOCKS and setting in the desired number using the HEX keypad numbers.

When TEST TIME has been selected in this field, the length of time that the test is to be run is entered in the field to the right of TEST TIME. In the example shown in Figure 3-8, a test length of 4 hours 35 minutes and 16 seconds has been entered through the use of the front panel keypad. The 5500A will stop the test after the selected time increment has elapsed. Entering 00:00:00 will result in a continous running test.

NOTE

The 5500A sends an automatic "Service Request" on the IEEE488 bus at the end of the test.

9. INJECT RATE - This line is a dual function line. The first choice the user has to make is the type of errors to be injected. This is accomplished by moving the cursor over the black area (where it says BPV INJ RATE in Figure 3-9) on the menu. The user then may select from the following:

BPV INJ RATE, F BIT INJ RATE, CRC INJ RATE, or D INJ(CRCrate) in ESF mode.

BPV INJ RATE, F BIT INJ RATE, or S BIT INJ RATE in D4 mode.

BPV INJ RATE or F BIT INJ RATE in SLC96 mode.

NOTE

The available inject modes are automatically restricted to those appropriate for the selected combination of FRAME and CLOCK SOURCE modes (refer to Table 3-3). Additional information on the inject modes can be found in the 5500A-628 option instructions in the options section of this manual.

Table 3-3. Error Injection Modes.

FRAME	CLK	BPV INJ	FBIT INJ	SBIT INJ	DATA INJ	CRC INJ
D4	INT	X	X	X		
D4	EXT	X	X	X		
D4	RX	X	X	X		
D4	THRU	X	X	X	X	

Table 3-3. Error Injection Modes.
(Continued)

FRAME	CLK	BPV INJ	FBIT INJ	SBIT INJ	DATA INJ	CRC INJ
D4	JIT(02)	X	X	X		
D4	THRU-J(JO2)	X	X	X	X	
D4	THRU+J(JO2)	X	X	X	X	
SLC™96	INT	X	X			
SLC™96	EXT	X	X			
SLC™96	RX	X	X			
SLC™96	THRU	X	X		X	
SLC™96	JIT(JO2)	X	X			
SLC™96	THRU-J(JO2)	X	X		X	
SLC™96	THRU+J(JO2)	X	X		X	
ESF	INT	X	X		X	X
ESF	EXT	X	X		X	X
ESF	RX	X	X		X	X
ESF	THRU	X	X		X	X
ESF	JIT(JO2)	X	X		X	X
ESF	THRU-J(JO2)	X	X		X	X
ESF	THRU+J(JO2)	X	X		X	X
UNFRAMED						
DISABLE	INT	X				
DISABLE	EXT	X				
DISABLE	RX	X				
DISABLE	THRU	X			X	
DISABLE	JIT(JO2)	X				
DISABLE	THRU-J(JO2)	X			X	
DISABLE	THRU+J(JO2)	X			X	

The second choice the user must make is selection of the inject error rate. The user programs the error rate by scrolling the half intensity block over the (----) INJ RATE value field. The user must select the mantissa of the rate desired using either the SELECT keys or the HEX keypad. The choices are 1 to 9. Then the user must use the CURSOR key to move the block to the right and change the exponent from -3 to -7 as desired.

10. LOGIC ERR RATE – The Model 5500A permits the user to inject single or multiple bit errors at rates from 9x10–3 to 1x10–9 errors/bit. The user programs the error rate by scrolling the half intensity block over the INJ ERROR RATE field. The user must select the mantissa of the rate desired using either the SELECT keys or the HEX keypad. The choices are 0 to 9. A 0 (zero) will disable the error inject. Then the user must use the CURSOR key to move the block to the right and change the exponent from –3 to –9 as desired. Once set, the rate is retained in non–volatile memory. Error injection is most often used for identification and testing the integrity of a circuit.

11. CLOCK SOURCE – There are seven (four without the J02 jitter option) possible selections for the source of the transmit clock timing for the "TX OUTPUT" of the 5500A–628 Module. These selections are; Rx, THRU, EXTERNAL, INTERNAL, **JIT, THRU–J**, and **THRU + J**. The clock sources listed in bold are only available with the J02 jitter option. Table 3–4 presents detailed information on each clock source.

Table 3–4. Clock Source Selections for ESF T1

CLOCK SOURCE	DESCRIPTION
INTERNAL	Internal Oscillator (main chassis/not in module) Select INT CLK for any standalone equipment testing and anytime loop timing is not appropriate (someone in the network must originate the clock; everyone cannot slave to recovered clock).
Rx	"RX INPUT" recovered clock Select RX CLK anytime the "TX OUTPUT" is required to be "loop timed" to the "RX INPUT" clock.
EXTERNAL	TTL input via pins 15 (EXT CLK) and 36 (RETURN) of the 40 pin "TEST ACCESS I/O" connector. Connect any TTL external clock source @ 1544000 + /–300 Hz for frequency tolerance testing of receivers, repeaters, etc. Connect any TTL precision clock, or network stratum 1 clock, etc., for use as: A) "TX OUTPUT" timing clock, and/or B) CSLP reference clock.

Table 3-4. Clock Source Selections for ESF T1 (Continued)

CLOCK SOURCE	DESCRIPTION
JIT	The JO2 OPTION modulates the internal clock source as specified via the Jitter Option Menu. The amplitude and frequency of phase modulation (and modulation wave shape - sine, triangle, or external modulation source) may be controlled to evaluate the jitter tolerance of network components.
THRU	"RX INPUT" bit stream is retransmitted at "TX OUTPUT" with all data bits, frame bits, data link bits, bipolar violations, etc. unaltered. This mode may be used to provide an in line repeater function (ALBO phase compensation, clock recovery, & retransmission of a nominal 6V peak-to-peak signal with 10%-30% trailing edge overshoot per Pub 62411). This mode also provides for injection of data errors, frame errors, etc. in live traffic for evaluation of error tolerance of command/response protocols, error checking algorithms, packet switching protocols, etc. (when the standard BERT pseudorandom test patterns are inappropriate).
THRU-J	Same as "THRU" above except the phase jitter (up to 10 unit intervals peak-to-peak) of the recovered "RX INPUT" clock is attenuated by approx. 40dB at 120 Hz (and above) to a level of less than .1 unit intervals peak-to-peak. This de-jittered clock is then used as the "TX OUTPUT" clock source. This mode may be used to sectionalize jitter tolerance problems, especially when the standard BERT pseudorandom test patterns are inappropriate and/or when extended out of service testing and troubleshooting is not permitted.
THRU + J	Same as "THRU" and "THRU-J" above except the "jitter attenuated", recovered "RX INPUT" clock is phase modulated as specified via the JO2 jitter option menu, and then used as the "TX OUTPUT" clock source. This mode may be useful in characterizing the jitter tolerance margins (or shortcomings) of network components in "live traffic" situations.

12. AUTO RESYNC - The auto resync function in the 5500A has three states; enable, disable, and timed. When the auto resync feature is disabled, the 5500A will continue to count bit errors once synchronization has been obtained, regardless of the number of bit errors per unit time.

When the auto resync is enabled, the 5500A obtains synchronization and then

continually monitors the bit error count and, when the bit error rate exceeds a predetermined threshold, the 5500A will declare it has lost synchronization and will not recover synchronization until a preset number of bits matches the pattern, usually set at 56 bits. During this time the 5500A is out of synchronization, error parameter collection is suspended, with only the time the unit is out of synchronization being accumulated.

In the timed resync mode, a number of 10 millisecond intervals (0–999, representing 0 to 9.99 seconds) is selected by the user as the time span of an internal timer. During the time cycle, if at least one bit error occurs during each 10 millisecond interval, the 5500A will count these errors until the timer runs out. When the timer runs out, the 5500A will check the bit error sync threshold to determine if sync should be broken. If the 5500A breaks sync, it will enter the auto resync disable mode and restart the internal timer. During the timer period, two events are taking place; 1) the 5500A is continuing to accumulate bit errors and, 2) the 5500A is monitoring the data to determine if errors have ceased. If only one 10 millisecond interval is error free, the timer is reset. If errors have ceased, the 5500A continues and the timer is reset, awaiting the next bit error occurrence.

13. TX ENA BDG/MON –The TX OUTPUT jack is connected, tip and ring, to the secondary winding of the 628 transmitter output transformer via series relay contacts. The relay contacts are normally closed only in the "TERM" mode and open in the "BRDG" and "MON" modes (and open anytime "LOOP" is enabled). The "TX ENA BRDG/MON" ENABLE/DISABLE option allows the TX relay to be enabled or disabled in the Bridge and Monitor modes. The sleeve is connected to the test set "ground" circuit for shield termination.

14. USER PA SYNC – The user pattern sync mode may be off, frame, or superframe. These user pattern sync modes are provided for those test applications where you must be able to control bit patterns in specific channel time slots of the T1 signal.

The frame mode will align a 24 byte user data pattern with T1 frame sync so that byte one of the user pattern is transmitted in the first time slot of the framed T1 signal, and byte two is the second slot and so on.

The superframe mode will align a 288 byte pattern or 576 byte pattern for ESF, with D4 or SLC™96 superframe sync. the first 24 bytes go out in frame one of a superframe. The second 24 bytes go out in frame two, and so on. User patterns 1 thru 3 are limited to 135 bytes, so you must test with User Pattern 4 to test with superframe patterns. In this mode and the frame mode the 4th, 5th, and 6th bytes of the user pattern are used for BERT sync and must be unique.

In some applications you may need short patterns, such as special non–standard loop–up and loop–down codes for CSUs, repeaters, or other network equipment. to send these short patterns set the user pattern sync to "OFF". the pattern will be sent repeatedly without frame alignment. In this mode the first three bytes of the user pattern are used for receive–user–pattern–sync and must be unique.

3.3.4 BERT Results/Parameters Menu

The primary purpose of the BERT results/parameters menu is to view the results of a test, either as the test is running and/or when the test is completed. The 5500A monitors and keeps track of over 45 parameters simultaneously depending upon the interface module installed.

To view the BERT Results/Parameters menu, follow these steps:

1. Perform the initial power up procedure in paragraph 3.3.

2. Bring the menu matrix help menu to the screen as instructed in paragraph 3.4.1.

3. Press the 1 key on the keypad.

4. Press the GO TO softkey.

5. The BERT Results/Paramters menu should now be on the display.

3.3.4.1 RS-232 BERT Results/Parameters Menu

There are three softkeys for this menu. Their functions are as follows:

The top softkey (refer to Figure 3-10) is a reflection of the SYNC and SYNC REC LEDs on the front panel. When the 5500A is in the RUN mode, the top softkey will display BRK until sync is acquired. When sync has been acquired, the SYNC LED will turn on and the softkey will display SYNC. At this point in time, the softkey may be pressed to force a sync break if desired. If the 5500A looses sync, the SYNC LED will turn off and the softkey will display LOS (loss of sync). When the 5500A recovers sync, the SYNC REC LED and the SYNC LED will be turned on and the softkey will display REC. At this time pressing the softkey will reset the SYNC REC LED (turning it off) and change the softkey display to SYNC.

The second softkey (INJ) is used to turn the error injection on (INJ highlighted) or off (INJ as shown in Figure 3-10).

The third softkey (CLR) is used to clear all the parameter counters and reset all the displays to zero. Pressing the CLR softkey will result in the display changing to 'OK?'. This is to prevent accidental erasure of test data. To clear the parameters the user must press the softkey again before the "OK?" is replaced with CLR (about 2 seconds).

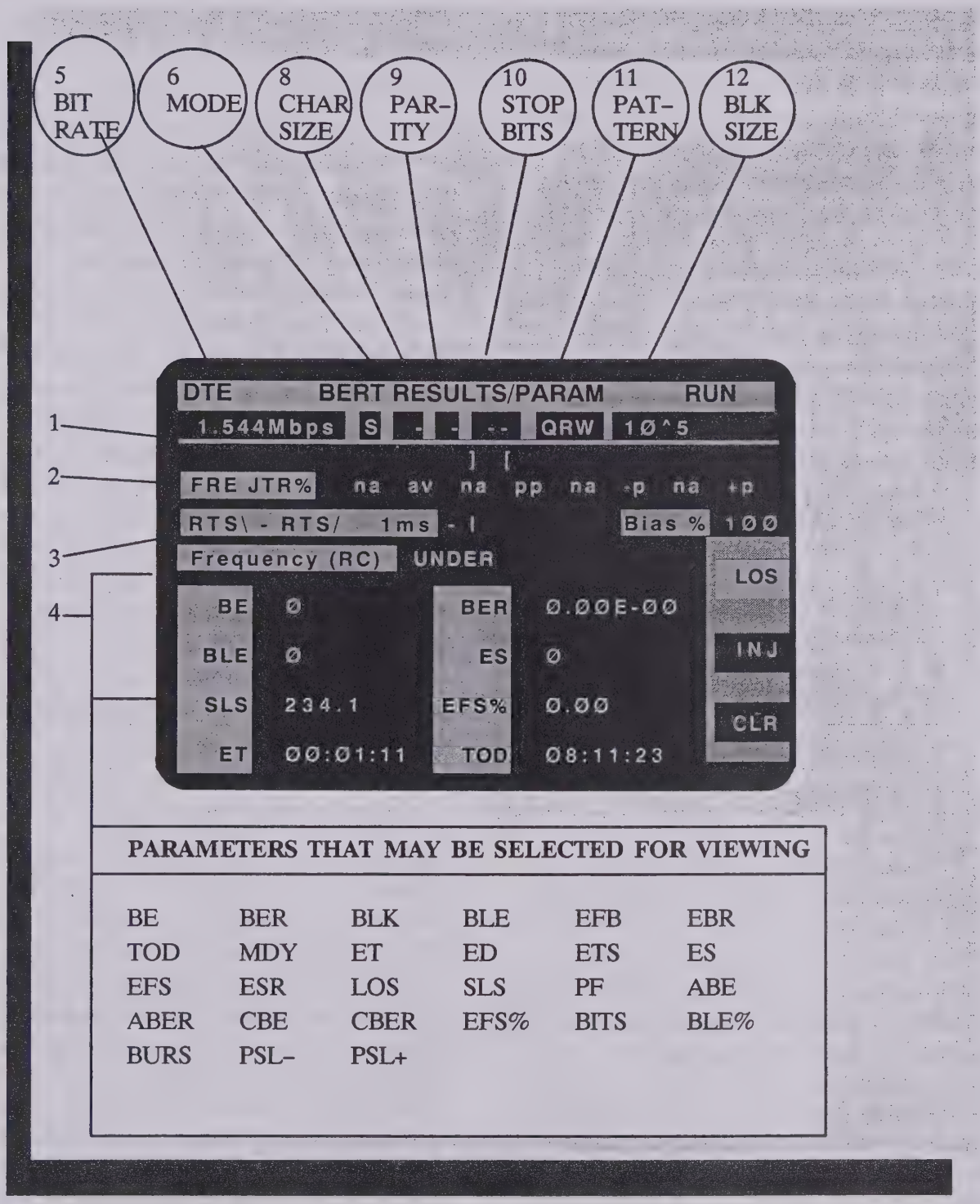
The top line of this display identifies the menu, shows if DTE or DCE has been selected, and if the 5500A is in the RUN mode. The second line is a condensed version of the BERT format menu discussed in section 3.3.2.1 The circled numbers in Figure 3-10 refer to the step number in paragraph 3.3.2.1 that refers to that specific area of the display. The name of the display line is also included in each circle. By moving the cursor over any of these areas, it is possible to change that selected value just as if it were being accomplished on the BERT format menu.

For example, if the cursor were located as shown in figure 3-9 (over Ext Clk), pressing the CURSOR SELECT keys would change the bit rate selection to one of the values shown in Figure 3-8.

The remaining lines of the display are:

1. FRE JTR % - This line is used to display the results of the low speed (75 to 72000 bps) jitter measurements. The line displays four different readings (all as a percent of bit period).

   The 5500A uses a sampling technique to measure edge timing differences on the received data. The received data is sampled at approximately 250 times the bit rate.



RS–232 BERT Results/Parameters Menu
Figure 3–10

The result of this sample is used to synchronize an internal clock to the average data transitions. Edge jitter is then calculated by measuring the percent of difference between the actual transitions of the received data and the transitions of the synchronized internal clock.

It should be noted that this sampling technique depends on transitions to achieve accuracy and synchronize the internal clock. Therefore, data with a 50% ratio of mark to spaces will result in the most accurate readings, while a long string of zero's would introduce errors.

The four readings that appear on this line are:

pp Represents peak–to–peak or the largest differences in edges during 1024 samples at frequencies above 300 bps or 256 samples below 300 bps.

+ p Represents the largest difference in data edges that is later than the internal oscillator.

– p Represents the largest difference in data edges that is earlier than the internal oscillator.

av Represents the average difference between data edges, sampled over the same bit period as **pp**, **+ p**, and **– p**.

The values that appear on this line will be numeric, 0–99, if the frequency of the receive data is between 75 and 72000 bps. If the receive data is outside the frequency range, a *na* will appear as the value.

The only operator selection available on this line is **FRE** or **HLD**. The selection is made by placing the cursor over the first field in this line (FRE or HLD) and pressing either select key to toggle between FRE and HLD.

2. The measurement of the time interval between two specific events is required for some test applications. This line on the BERT menu permits the user to select the events from the following; TD (transmit data), RD (receive data), CTS, RTS, DCD, DSR, DTR, or SQ and DLY (network loop delay). The network loop delay can measure on a single transmission (SNGL) or continuously (CONT). On the other measurements, the user may further select where the measurement is to take place; the leading or rising edge of the pulse (/) or the trailing or falling edge of the pulse (\). The time interval scale is the next item to set. This value is 1, 10, or 100 us, 1, 10, or 100 ms, or 1, 10, or 100 seconds. The numeric value in the field is then multiplied by the scale factor to obtain the time interval between the two events.

3. Frequency (RC) – This line is used to measure the frequency of receive clock (RC), transmit clock (TC), external clock (XC), or the asynchronous bit rate (BR). The actual frequency being measured will appear in the field unless the frequency is below 150 Hz in which case the field will display UNDER.

4. There are eight windows available to the user to display any of the parameters listed in Figure 3–10. The 5500A keeps track of all the parameters simultaneously and the user may scroll between any or all of them in these windows, at any time, without disrupting the test in progress.

3.3.4.2 ESF T1 BERT Results Menu

The three softkeys for this menu (refer to Figure 3-11) perform the same functions as they do on the RS-232 BERT Results/Parameters menu and are explained in paragraph 3.3.3.1.

The top line of this display identifies the menu, shows what termination mode has been selected, and if the 5500A is in the RUN mode. The second line is a condensed version of the ESF T1 BERT setup menu discussed in section 3.3.2.2. The circled numbers in Figure 3-11 refer to the step number in paragraph 3.3.2.2 that refers to that specific area of the display. The name of the display line is also included in each circle. By moving the cursor over any of these areas, it is possible to change that selected value just as if it were being accomplished on the T1 ESF BERT SETUP menu.

For example, if the cursor were located over clock source, pressing either of the **CURSOR SELECT** keys would change the CLOCK SOURCE selection to one of the seven available choices.

The remaining lines of the display are:

1. This line is used to display the network loop delay. Network loop delay is measured by sending a bit error from the 5500A through the network to the distant end. The distant end is set to loop the bit error back through the network to the 5500A. The 5500A measures the time it takes from initial transmission of the bit error to the return of the bit error to the 5500A and displays that total time as network loop delay. The network loop delay timer can measure times up to 17 minutes and can display the loop times in 1 usec, 10 usec, .1 Msec, 1 Msec, or 10 Msec resolution.

2. Frequency (RC) - This line is used to measure the frequency of receive clock (RC), transmit clock (TC), or external clock (XC). The actual frequency being measured will appear in the field unless the frequency is below 150 Hz in which case the field will display UNDER.

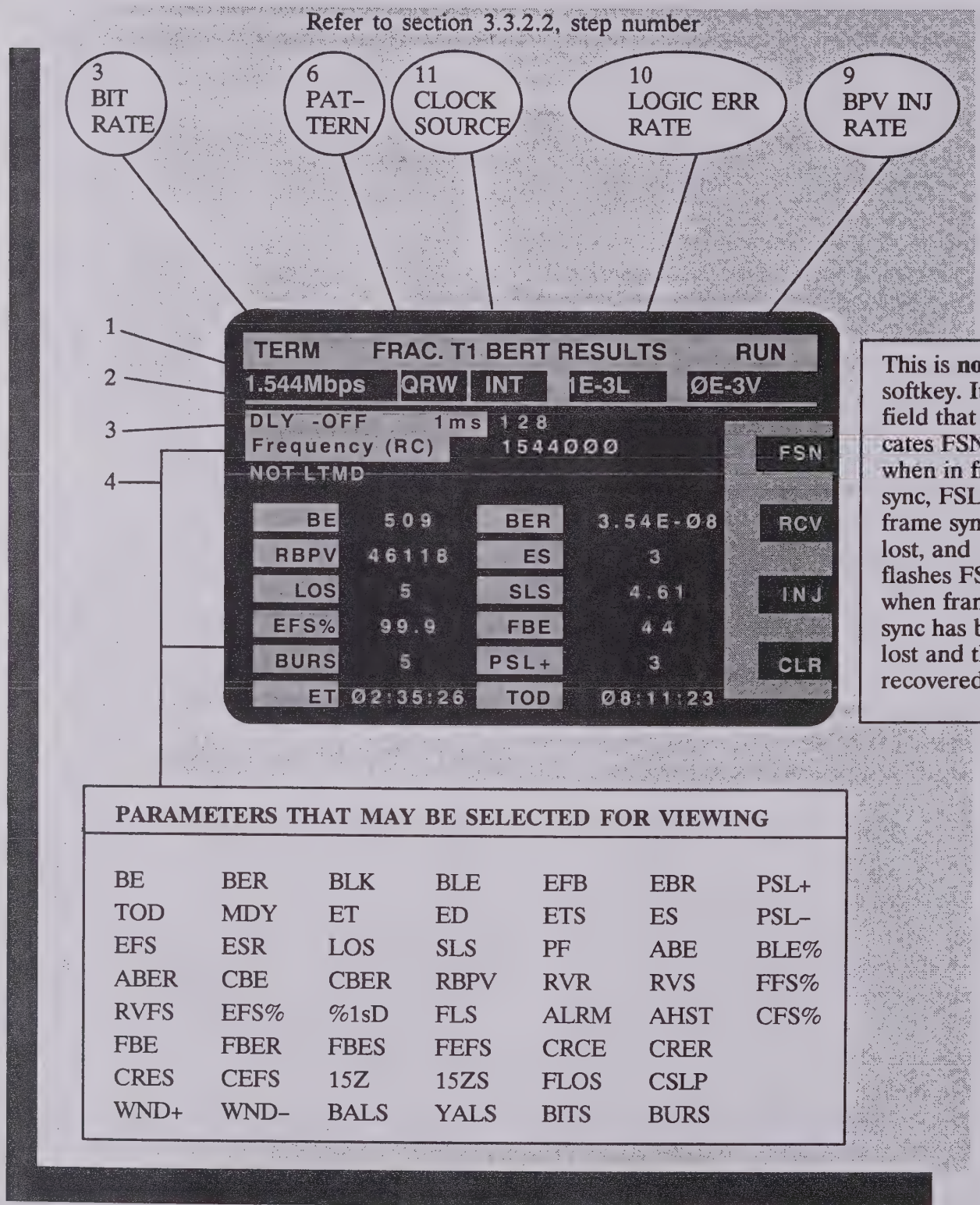
3. This line is used in conjunction with the clock slip (CLSP) measurement. As long as CLSP remains within the range of plus or minus 40 unit intervals, the LTMD (loop timed) indication will be displayed in this field. When CLSP exceeds this range, the flashing NOT LTMD (not loop timed) indication will appear in this field.

4. There are twelve windows available to the user to display any of the parameters listed in Figure 3-11. The 5500A keeps track of all the parameters simultaneously and the user may scroll between any or all of them in these windows, at any time, without disrupting the test in progress.

3.3.5 Printer Setup Menu

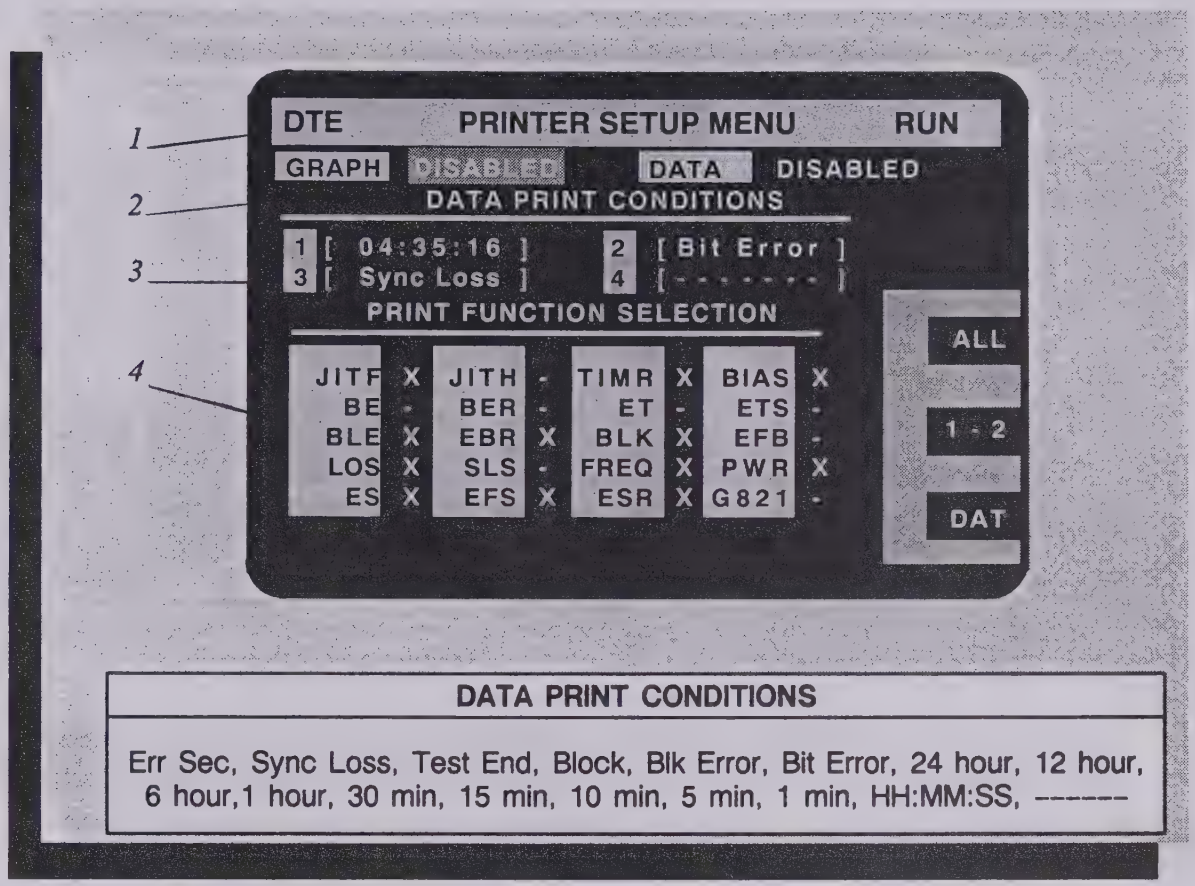
The printer setup menus, illustrated in Figure 3-12 and Figure 3-13, are used in conjunction with an optional printer to provide the user with time and date stamped hard copy of test results. The only difference between the RS-232 Printer Setup Menu and the ESF T1 Printer Setup Menu, is the number of parameters available for printing and the conditions under which a printout can take place.

The softkeys for these menus are used to control what is to be printed. The top two keys, ALL and 1-2, are used when a graph is to be printed. Pressing the ALL softkey commands the printer to print the entire graph. Pressing the 1-2 softkey instructs the printer to print only that section of the graph that appears between cursor #1 and cursor #2 (see



This is **not** a softkey. It's a field that indicates FSN when in frame sync, FSL when frame sync is lost, and flashes FSN when frame sync has been lost and then recovered.

T1 ESF BERT Results Menu
Figure 3-11


1
2
3
4
DTE
PRINTER SETUP MENU
RUN
GRAPH
DISABLED
DATA
DISABLED
DATA PRINT CONDITIONS
1 [04:35:16]
2 [Bit Error]
3 [Sync Loss]
4 [- - - - - - -]
PRINT FUNCTION SELECTION
JITF X JITH - TIMR X BIAS X
BE - BER - ET - ETS -
BLE X EBR X BLK X EFB -
LOS X SLS - FREQ X PWR X
ES X EFS X ESR X G821 -
ALL
1-2
DAT
DATA PRINT CONDITIONS
Err Sec, Sync Loss, Test End, Block, Blk Error, Bit Error, 24 hour, 12 hour, 6 hour,1 hour, 30 min, 15 min, 10 min, 5 min, 1 min, HH:MM:SS, ------

RS-232 Printer Setup Menu
Figure 3-12

section 3.3.7 for information about the graph display). The final softkey, the DAT key, is used to instruct the printer to print the numeric data.

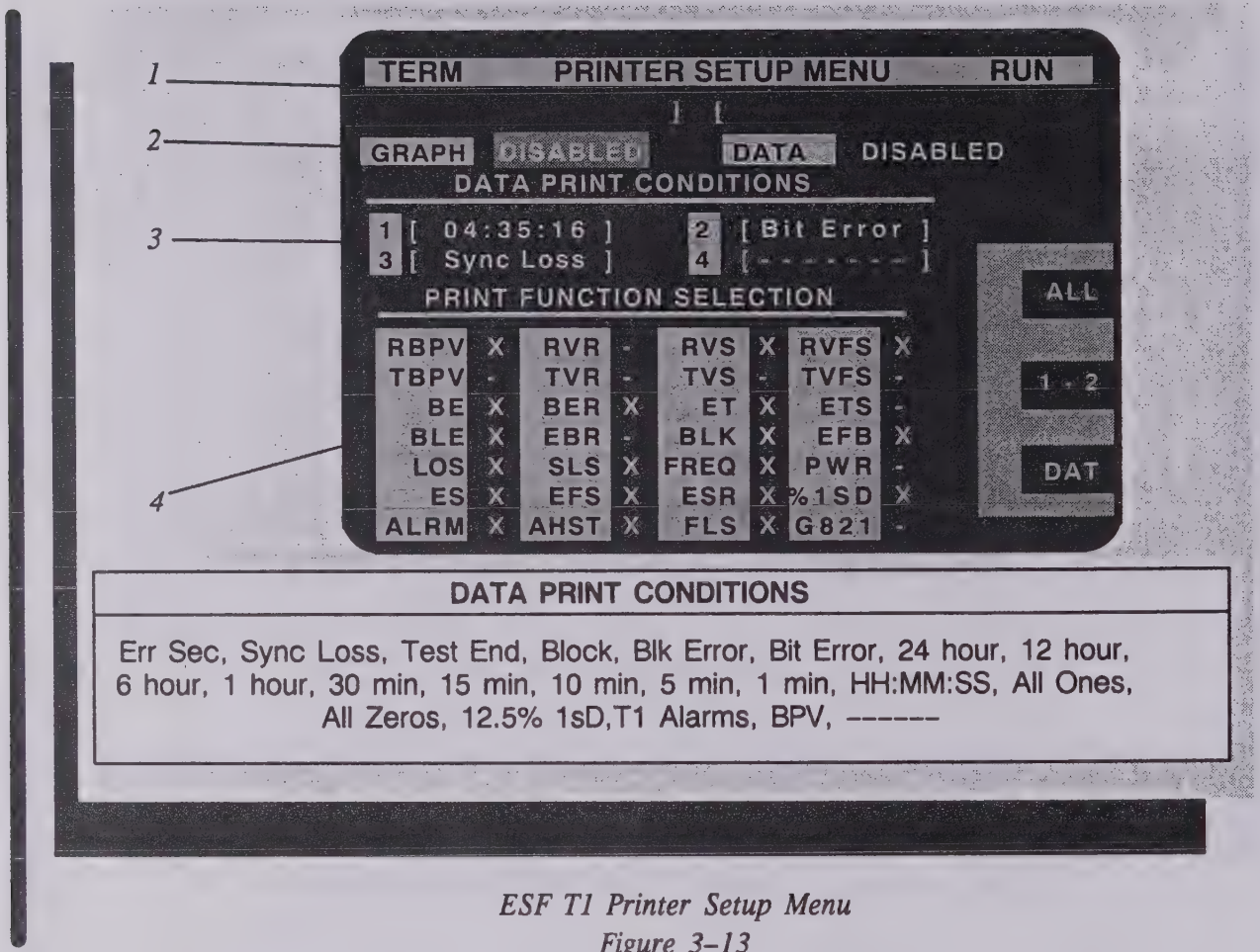
The explanation for each of the keyed areas in Figure 3-12 and Figure 3-13 follows:

1. This line is the same as the previous menus.

2. This area of the display is used to ENABLE or DISABLE the graph printout functions. Place the cursor in the field to the right of GRAPH and use the CURSOR SELECT keys to select ENABLE or DISABLE.

This area of the display is also used to ENABLE or DISABLE the data printout functions. Place the cursor in the field to the right of DATA and use the CURSOR SELECT keys to select ENABLE, ENB-ALRM, or DISABLE. The ENB-ALRM position sounds an audible alarm each time the print function is enabled.

3. This area of the menu, the DATA PRINT CONDITIONS, is used to select 1, 2, 3, or 4 conditions under which a print out will take place. In the example shown in Figure 3-12, a printout will occur every 4 hours, 35 minutes, and 16 seconds (line 1), every time there is a bit error (line 2), and every time there is a sync loss (line 3). The available print conditions are listed in


1
2
3
4
TERM
PRINTER SETUP MENU
RUN
GRAPH DISABLED
DATA DISABLED
DATA PRINT CONDITIONS
1 [04:35:16]
2 [Bit Error]
3 [Sync Loss]
4 [- - - - - - -]
PRINT FUNCTION SELECTION
RBPV X RVR - RVS X RVFS X
TBPV - TVR - TVS - TVFS -
BE X BER X ET X ETS -
BLE X EBR - BLK X EFB X
LOS X SLS X FREQ X PWR -
ES X EFS X ESR X %1SD X
ALRM X AHST X FLS X G821 -
ALL
1 - 2
DAT
DATA PRINT CONDITIONS
Err Sec, Sync Loss, Test End, Block, Blk Error, Bit Error, 24 hour, 12 hour, 6 hour, 1 hour, 30 min, 15 min, 10 min, 5 min, 1 min, HH:MM:SS, All Ones, All Zeros, 12.5% 1sD,T1 Alarms, BPV, ------

ESF T1 Printer Setup Menu
Figure 3-13

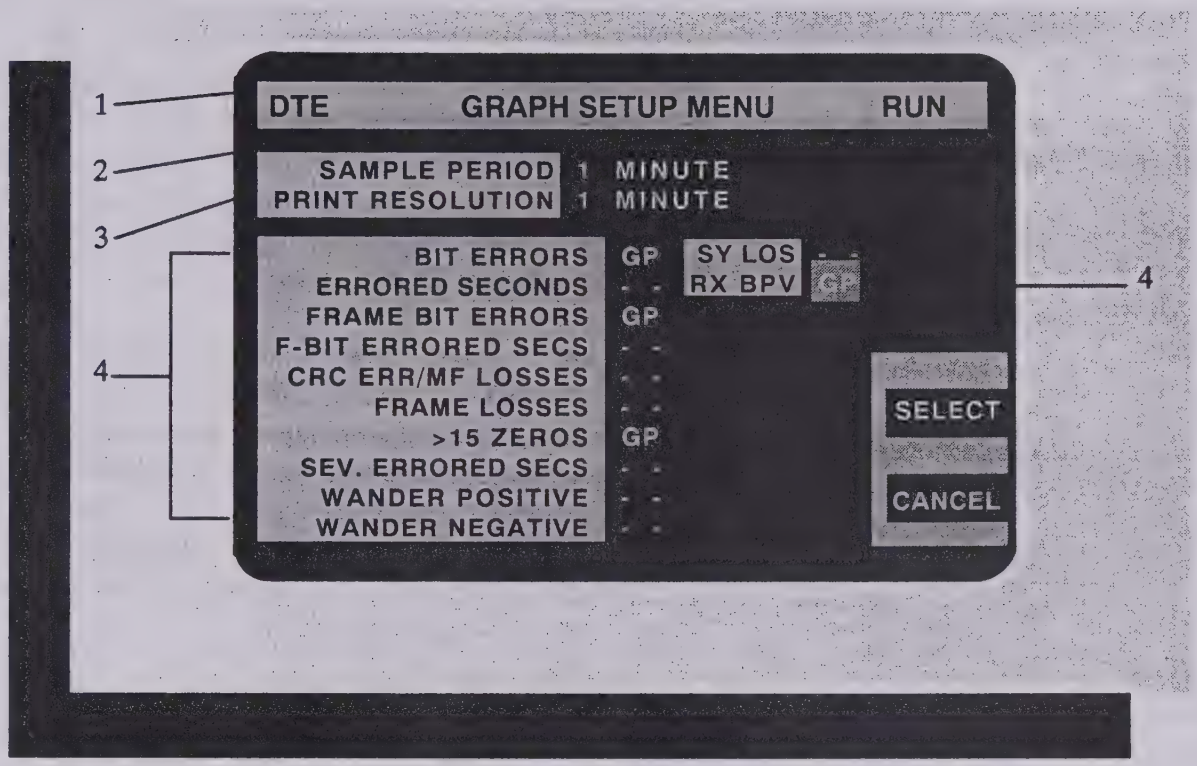
Figure 3-12 and Figure 3-13. In addition to the pre-programmed times on which a printout will take place, the user may select anytime period by using the HH:MM:SS format in one of the fields and entering the desired frequency for a printout in hours, minutes, and seconds.

4. This area of the display, the PRINT FUNCTION SELECTION, is used to select those parameters the user wishes to have on the printed results. An "X" after the parameter indicates that that parameter has been selected to be printed. Selection is made by placing the cursor opposite the desired parameter, over the X or -, and using the CURSOR SELECT keys to enable (X) or disable (-) the printing of the parameter.

3.3.6 Graph Setup Menu

The Graph Setup Menu is shown in Figure 3-14.

The softkeys for this menu are used to change the previous graph data selection to the current selection. The SELECT softkey will activate any changes that have been made on this menu and discard any stored graph data while the CANCEL softkey will cancel any changes that have been made without discarding the stored graph data.



Graph Setup Menu
Figure 3–14

The softkey labels (SELECT and CANCEL) will flash to indicate that the stored configuration and the graph data do not match the displayed configuration.

The explanation for each of the keyed areas in Figure 3–14 follows:

1. The top line of the display is the same as in previous menus.

2. The SAMPLE PERIOD field defines the sample resolution for the stored graph data. The resolutions available are 1 second, 10 seconds, 1 minute, 10 minutes, and 1 hour. Graph data can then be displayed at the selected period or the next 2 resolutions (selection is made on the Graph Display Menu, section 3.4.7).

3. The PRINT RESOLUTION field defines the resolution of the printed graph data. The graph can be printed at the sample period or the next two resolutions as summarized below:

Sample Resolution	Print Period
1 second	1 or 10 seconds 1 minute
10 seconds	10 seconds 1 or 10 minutes
1 minute	1 or 10 minutes 1 hour
10 minutes	10 minutes 1 hour
1 hour	1 hour

4. The parameter field permits the user to select the parameter(s) to be graphed (G), graphed and printed (GP) or not selected

for either (--). Selection is made by placing the cursor opposite the desired parameter and using the CURSOR SELECT keys to choose G, GP, or --.

3.3.7 Graph Display

The GRAPH DISPLAY located at the left of the BERT DISPLAY in the menu matrix provides the user with an important tool in locating the source of a problem.

Often, the cause of a burst of errors may be related to its time occurrence. That is, a large air conditioner or other high power device may cycle on and the surge may cause a nearby terminal or modem to suffer a power line hit. The events can be correlated to the cause using the GRAPH DISPLAY.

The operator may choose to plot up to four different error parameters versus time so as to generate a more complete picture of circuit conditions.

A typical graph display of bit errors is shown in Figure 3-15. A typical test set up might involve graphing bit errors, sync losses, bipolar violations (T-Carrier testing), and errored blocks. Other parameters can be graphed but generally speaking, the above are the most important in isolating problems.

The graph display stores up to sixty hours of data in up to one minute intervals if only one parameter is graphed. This permits long term unattended testing (over a weekend for example) without losing the data, or when it occurred.

When setting up a GRAPH DISPLAY for a long term test it is suggested to set the HORIZONTAL time scale to sixty minutes per division and the VERTICAL scale to x1 for the maximum sensitivity. This will cause even single events to be displayed. When the user wishes to view the display the scales can always be changed for a more convenient display. No data is lost by changing the scales.

The user also can print out the graphic data (for a single parameter). The Model 5500A will print out data continuously in 1, 10, or 60 minute increments depending upon the horizontal scale setting and the user can therefore bypass the 60 hour limitation of the GRAPH DISPLAY itself.

Figure 3-13 and Figure 3-14 detail the setup for graph data (GRAPH DATA SELECTION). Figure 3-15 details the actual graph display and display controls. Table 3-5 presents the graph definitions. The Model 5500A graph is provided only under local control. For remote control operation, an intelligent controller may be utilized to obtain data plots.

The Graph Display Menu, illustrated in Figure 3-15, displays a single graph for any of the data types selected on the Graph Data Selection menu. This menu does not have any softkeys associated with the display.

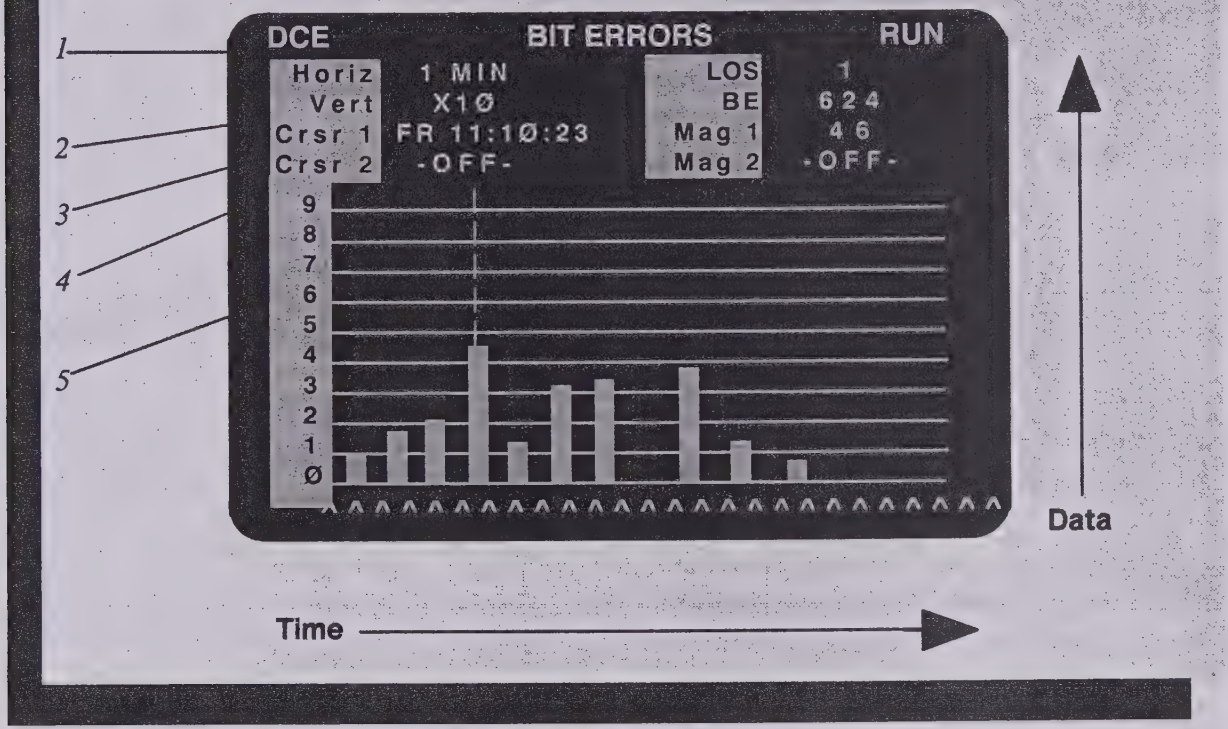
The explanation for each of the keyed areas in Figure 3-15 follows:

1. The top line of this display is different in that the title of the menu does not appear in the top center. Instead, the top center of this menu is used to display the parameter being graphed from the the list of those selected on the Graph Data Selection menu. The choice of which parameter to view is made by positioning the cursor over the function displayed at the top of the display and then using the CURSOR SELECT keys to scroll to the desired parameter. The remainder of the top line of this display is the same as the previous displays.

2. The Horiz field is used to select the time scale factor based upon the SAMPLE PE-

Parameters That Can Be Viewed in Fields Above Mag1			
WITH RS–232 MODULE INSTALLED			
BITS	EFS%	CBER	CBE
ABER	ABE	PF	SLS
LOS	ESR	EFS	ES
ETS	ED	ET	MDY
TOD	EBR	EFB	BLE
BLK	BER	BE	

WITH ESF T1 MODULE INSTALLED			
ALL OF THE PARAMETERS LISTED ON LEFT PLUS:			
YALS	BALS	WND–	WND+
CSLP	FLOS	15ZS	15Z
CEFS	CRES	CRER	CRCE
FEFS	FBES	FBER	FBE
AHST	ALRM	FLS	%1sD
RVFS	RVS	RVR	RBPV



Graph Display
Figure 3–15

RIOD selection made on the Graph Data Selection menu.

Table 3-5. Graph Definitions.

SYMBOL	DEFINITION
Crsr 1	The main cursor for the graph used to determine the exact time and magnitude of the data being plotted. The UP SELECT key advances the cursor in the time increments set by the horizontal resolution. The DOWN SELECT key backs up the cursor in time. A time of day clock reading is provided next to the Crsr 1 display.
Crsr 2	Cursor 2 is used for the plot printing function. Data between Cursor 1 and Cursor 2 can be printed out by depressing the SOFTKEY corresponding to 1-2 in the PRINT SELECTION menu.
Horizontal (Horiz)	CRT field that displays the time scale selected. One, ten or sixty minutes per division may be selected. Thirty time divisions can be displayed without scrolling to the right. The resolution decreases as the number of parameters to be graphed increases.
Vertical (Vert)	CRT field that displays the vertical scale factor. Factors from 1 to 100,000 are provided.
Mag 1	Displays the magnitude of the data at Cursor 1 position.
Mag 2	Displays the magnitude of the data at Cursor 2 position.
ALL	Softkey used to print entire sixty hour graph plot. Will also enable continuous printout of graph data.
1-2	Prints graph data between Cursor 1 and 2 only.
DAT	Softkey used to select numerical data print out instead of graphic data. Used with any standard RS-232 interface printer.
Top Line Center of graph display	CRT field used to select data parameter(s) to be plotted.

NOTE

The graph data buffer is approximately 5400 samples long. Data is collected and stored until the buffer is full and then the oldest sample(s) are discarded as required to make room for new samples. The period of time that is represented by data in the buffer is a function of the sample period and the number of data types to be sampled. For example, assume a sample period of 10 seconds with three data types selected. To compute buffer length:

Buffer length = (5400/3)*10 = 18,000 seconds = 5 hours

3. The Vert field selects the vertical resolution for the displayed graph. The vertical resolution selects a magnitude multiplier corresponding to the labels on the left side of the display.

4. The Crsr 1 and Crsr 2 define the day-of-the-week, hour, and minute of the samples at cursors 1 and 2. The two cursors may be used to print a section of the graph data. Cursor 2 may be off; if not, cursor 1 always precedes cursor 2.

5. The Mag 1 and Mag 2 fields display the magnitude of the data at cursors 1 and 2.

6. The two fields above the Mag 1 field are used to display the numeric results of a selected parameter (these parameters are not controlled by the parameters on the Graph Data Selection menu). To select the desired parameter, move the cursor to either field and use the CURSOR SELECT keys to select the desired parameter. The parameters available are listed in Figure 3-15.

3.3.8 RS 232/IEEE488 Menu

The RS 232/IEEE488 Menu, illustrated in Figure 3-16, is used to configure the 5500A remote ports to match the device to be connected to the port, ie., a printer or terminal.

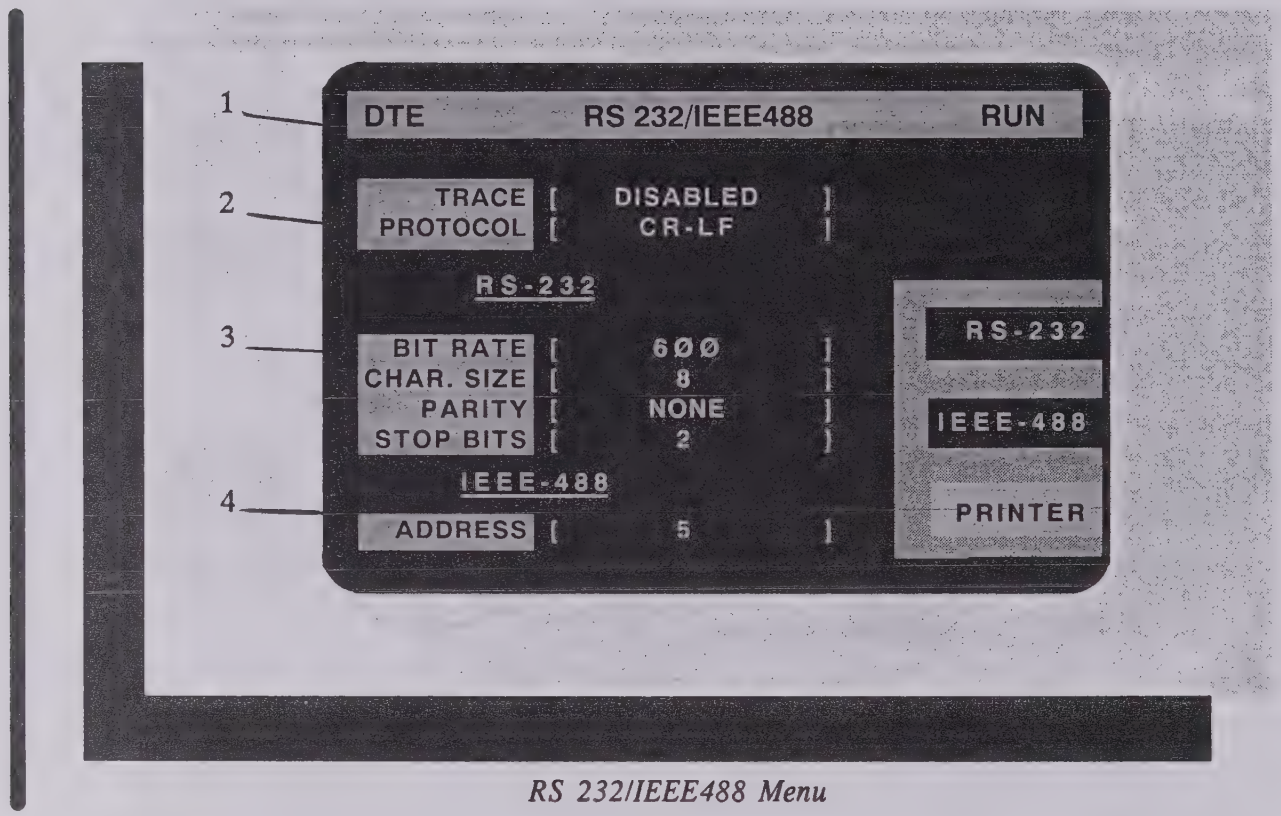
The softkeys for this menu are used to select RS-232, IEEE-488, or PRINTER. If RS-232 operation is going to be used, the user presses the RS-232 softkey if a terminal or modem is to be connected to the 5500A RS-232 remote port. If a direct printer connection is to be made via the RS-232 remote port, the PRINTER softkey is pressed. When the parallel IEEE-488 (sometimes referred to as GPIB or HPIB) remote port is to be used, the IEEE-488 softkey is pressed.

The explanation for each of the keyed areas in Figure 3-16 follows:

1. The TRACE field is used to view the character stream between the 5500A and the remote device over the remote port for possible trouble-shooting. When the TRACE is ENABLED, the user will observe the data stream going to the remote device on the right half of the line and the data stream coming from the remote device on the left side of this line of the display. The trace will also be visible on all the other menus that have the trace brackets "] [" on the second line of the display.

2. The PROTOCOL field is used to select the controller response format. The choices are CR-LF and ACK-NAK.

3. This area of the menu is used to select the various RS-232 protocols. The bit rate is selectable from 50, 75, 110, 150, 300, 600, 1200, 2400, 4800, 7200, or 9600 bps. The character size may be 7 or 8 bits, parity of odd, even, or none, and stop bits of 1, 1.5, or 2. These are all selected by placing



RS 232/IEEE488 Menu
Figure 3–16

the cursor over the selected field and using the CURSOR SELECT keys to scroll to the desired value.

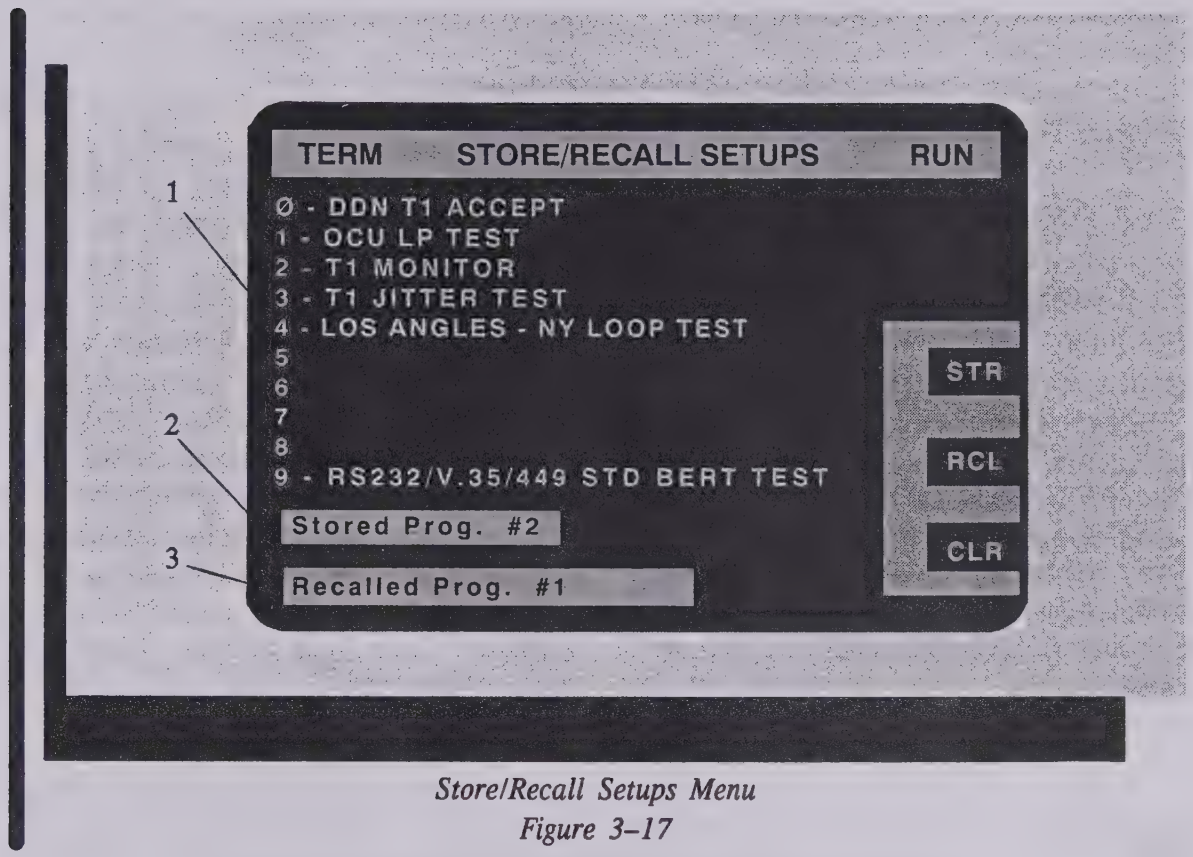
4. The IEEE–488 bus enables the simultaneous connection of up to 31 devices to a single controller. Each device on the bus has a numeric address (0 – 30). It is therefore necessary to "tell" the 5500A what it's address is so that it will respond to information sent to it. This line is used to set that address into the 5500A. Place the cursor over the address field and use the front panel keypad to enter the address.

3.3.9 Store/Recall Setups Menu

The Store/Recall Setups menu, illustrated in Figure 3–17, is used to store up to ten complete configuration setups thus making it much faster to repeat a recurring test at a later date.

The softkeys for this menu are used to store (STR), recall (RCL), or clear (CLR) a program area. The STR softkey stores the current setup in the memory location indicated by the cursor. The RCL softkey recalls the setup configuration stored in the memory location indicated by the cursor. The CLR softkey clears the program name from the menu field for the selected memory location but does not clear the memory location of the configuration setup.The front panel STORE and RECALL keys work in the same manner as the softkeys on this menu. To store a configuration into memory, follow these simple steps:

a. Setup the Model 5500A for the test desired.



Store/Recall Setups Menu
Figure 3–17

b. Press the STORE key.

c. Press the keypad number for the memory location into which this setup is to be stored. (The user may overwrite any previously stored configuration by simply storing a new configuration in the old location.)

d. Name the program following the procedure in #1 below.

To recall a program, follow these steps:

a. Press the RECALL key twice within 2 seconds.

b. Enter the number of the desired program using the front panel keypad.

The explanation for each of the keyed areas in Figure 3–17 follows:

1. The fields numbered 0 – 9 represent memory locations in which a particular configuration setup may be stored by the user. The field opposite the number is provided so that the user may assign a name to the program for ease in identification. The name may be typed in using a terminal or by placing the cursor over the character position and then use the CURSOR SELECT keys to scroll through the character set until the desired character is in place.

2. The Stored Prog field displays the number of the most recent program stored by the user.

3. The Recalled Prog field displays the number of the most recent program recalled by the user.

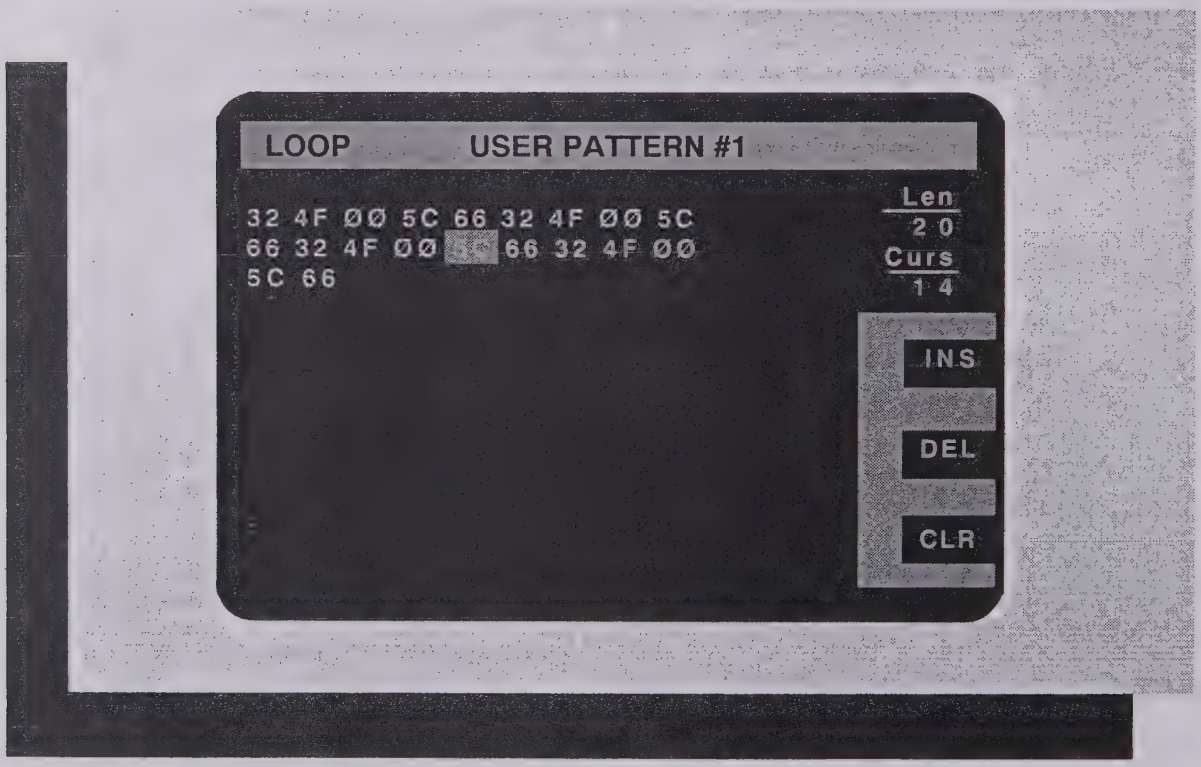
3.3.10 User Pattern Menu

The USER PATTERN display, Figure 3-18, allows the user to construct patterns for transmission by the Model 5500A. The USER PATTERN selection, when chosen, causes the Model 5500A to transmit a repetitive pattern of whatever the operator has placed in the USER PATTERN display. The user is permitted to enter up to 135 characters (2048 in User pattern 4) in HEX from the front panel HEX keypad or over the remote control ports. Each character in HEX is an 8 bit long word so the total bit length which could be input is 1080 bits. However, the user may enter as few as three characters if desired.

NOTE

If the RAM backup battery failed or has been replaced it is possible that the Model 5500A will, power up, default to the system menu and flash the USER PATTERN memory block. This "error" can be ignored or the user may choose to place three or four characters into the User Pattern display. These can be any HEX characters or the user may want to place an actual pattern into memory.

Placing a HEX pattern into a memory is a straight forward process. The user scrolls to the USER PATTERN display using the **MENU** keys. Then, beginning in the upper left hand corner, enters the desired HEX character from the HEX keypad.



User Pattern Menu
Figure 3-18

Using the right **CURSOR** key, advance the half intensity block to the next position and enter another character. Repeat this process for the pattern length desired.

The user may desire to input a pattern on a binary, bit by bit basis. This is a somewhat more complex procedure, but the following table and examples will serve to explain the procedure.

Table 3-6 contains the 256 possible HEX combinations and their binary equivalents.

Step 1: Write the pattern desired bit by bit in the following format with the first transmitted bit first. An example T1 set code pattern is shown below (a continual repeating 10000).

1 0 0 0 0 1 0 0 0 0 1 0 0 0 0 ------

Step 2: Table 3-6 is constructed so that the least significant bit (LSB) is the inverse of what normally would be expected. This is a reference to allow the user to easily "invert" the desired pattern.

Step 3: Segment the pattern into 8 bit bytes as shown below until the pattern repeats. In this example the pattern repeats after the fortieth bit.

10000100 00100001 00001000
01000010 00010000 10000100

Step 4: Compare the first byte (10000100) to the various bytes in Table 3-6 and note that it is identical to the pattern for the HEX character set "21".

Step 5: Compare the second byte (00100001) to the tabulated values and note that it is equivalent to HEX "84".

Step 6: Repeat the procedure for all the remaining bytes. The 40 bit long pattern equates to the HEX character string "21 84 10 42 08"

STEP 7: The repetitive 10000 pattern has thus been converted into its HEX pattern "21 84 10 42 08" into the USER PATTERN display and the pattern generated will be a continuous 1000010000-----.

NOTE

This sample pattern (10000) is the Set Code used to loop back a T-1 Channel Service Unit (CSU) such as the Phoenix Model 1544.

An example of another use is a pattern with a long string of 0's to stress test a regenerative repeater's clock recovery and reshaping capability. Let us assume that the user desires a string of 31 0's. It is necessary to have at least one "1" in the string so the pattern would look like:

10000000 00000000 00000000 00000000 100... etc

HEX 1 HEX 0 HEX 0 HEX 0

The user would enter the pattern in HEX as "10 00" and this would give a 31 zero transmission followed by a 1 and another string of 31 zeroes and so on. With practice the user can input almost any binary pattern desired. The only restriction being the pattern must be able to repeat within 2048 bytes.

3.3.11 BIG BERT Display

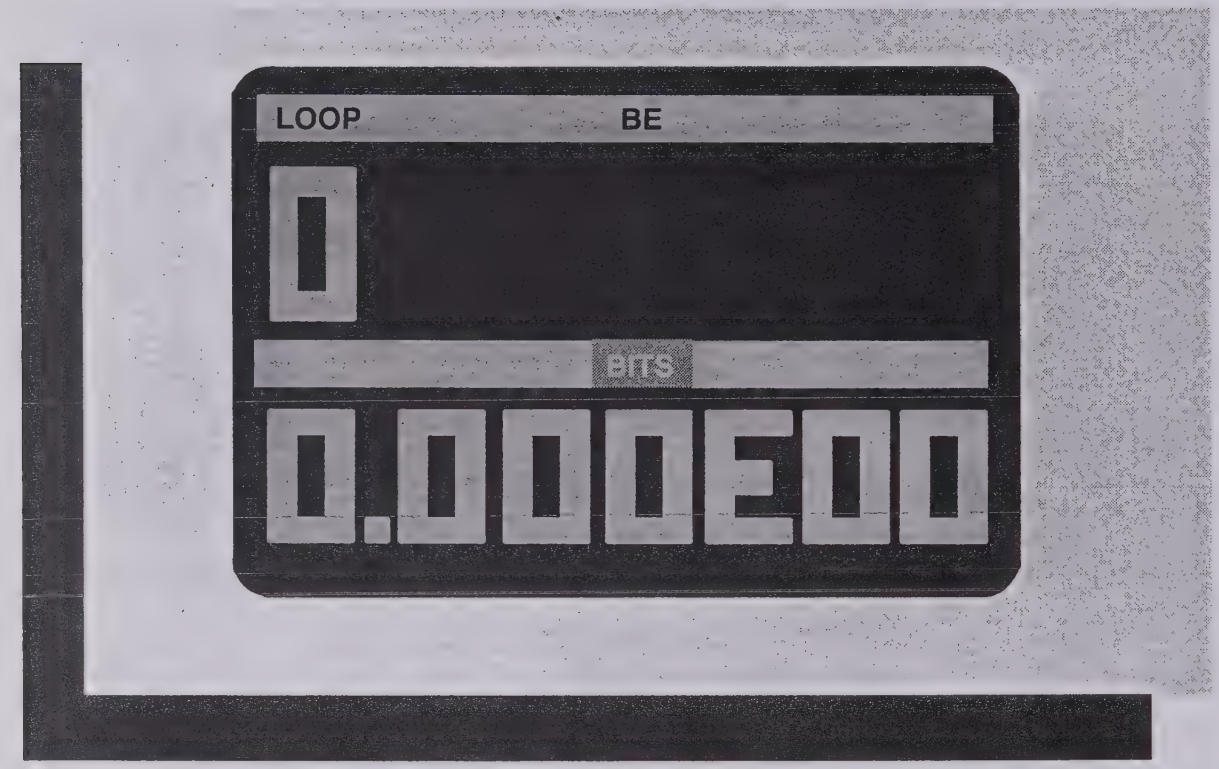
The BIG BERT DISPLAY located to the right of the MAIN BERT DISPLAY is provided as a convenience for the user. This menu allows the selection and display of any two of the error measurement parameters which are accumulated by the Model 5500A. The BIG BERT menu is a split screen, large format display as shown in Figure 3-19. The user may choose a parameter

Table 3-6. Hex to Binary Conversion.

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
00	00000000	50	00001010	A0	00000101
O1	10000000	51	10001010	A1	10000101
02	01000000	52	01001010	A2	01000101
03	11000000	53	11001010	A3	11000101
04	00100000	54	00101010	A4	00100101
05	10100000	55	10101010	A5	10100101
06	01100000	56	01101010	A6	01100101
07	11100000	57	11101010	A7	11100101
08	00010000	58	00011010	A8	00010101
09	10010000	59	10011010	A9	10010101
0A	01010000	5A	01011010	AA	01010101
0B	11010000	5B	11011010	AB	11010101
0C	00110000	5C	00111010	AC	00110101
0D	10110000	5D	10111010	AD	10110101
0E	01110000	5E	01111010	AE	01110101
0F	11110000	5F	11111010	AF	11110101
10	00001000	60	00000110	B0	00001101
11	10001000	61	10000110	B1	10001101
12	01001000	62	01000110	B2	01001101
13	11001000	63	11000110	B3	11001101
14	00101000	64	00100110	B4	00101101
15	10101000	65	10100110	B5	10101101
16	01101000	66	01100110	B6	01101101
17	11101000	67	11100110	B7	11101101
18	00011000	68	00010110	B8	00011101
19	10011000	69	10010110	B9	10011101
1A	01011000	6A	01010110	BA	01011101
1B	11011000	6B	11010110	BB	11011101
1C	00111000	6C	00110110	BC	00111101
1D	10111000	6D	10110110	BD	10111101
1E	01111000	6E	01110110	BE	01111101
1F	11111000	6F	11110110	BF	11111101
20	00000100	70	00001110	C0	00000011
21	10000100	71	10001110	C1	10000011
22	01000100	72	01001110	C2	01000011
23	11000100	73	11001110	C3	11000011
24	00100100	74	00101110	C4	00100011
25	10100100	75	10101110	C5	10100011
26	01100100	76	01101110	C6	01100011
27	11100100	77	11101110	C7	11100011
28	00010100	78	00011110	C8	00010011
29	10010100	79	10011110	C9	10010011
2A	01010100	7A	01011110	CA	01010011
2B	11010100	7B	11011110	CB	11010011
2C	00110100	7C	00111110	CC	00110011

Table 3–6. Hex to Binary Conversion (Cont.).

HEX	BINARY LSD	HEX	BINARY LSD	HEX	BINARY LSD
2D	10110100	7D	10111110	CD	10110011
2E	01110100	7E	01111110	CE	01110011
2F	11110100	7F	11111110	CF	11110011
30	00001100	80	00000001	D0	00001011
31	10001100	81	10000001	D1	10001011
32	01001100	82	01000001	D2	01001011
33	11001100	83	11000001	D3	11001011
34	00101100	84	00100001	D4	00101011
35	10101100	85	10100001	D5	10101011
36	01101100	86	01100001	D6	01101011
37	11101100	87	11100001	D7	11101011
38	00011100	88	00010001	D8	00011011
39	10011100	89	10010001	D9	10011011
3A	01011100	8A	01010001	DA	01011011
3B	11011100	8B	11010001	DB	11011011
3C	00111100	8C	00110001	DC	00111011
3D	10111100	8D	10110001	DD	10111011
3E	01111100	8E	01110001	DE	01111011
3F	11111100	8F	11110001	DF	11111011
40	00000010	90	00001001	E0	00000111
41	10000010	91	10001001	E1	10000111
42	01000010	92	01001001	E2	01000111
43	11000010	93	11001001	E3	11000111
44	00100010	94	00101001	E4	00100111
45	10100010	95	10101001	E5	10100111
46	01100010	96	01101001	E6	01100111
47	11100010	97	11101001	E7	11100111
48	00010010	98	00011001	E8	00010111
49	10010010	99	10011001	E9	10010111
4A	01010010	9A	01011001	EA	01010111
4B	11010010	9B	11011001	EB	11010111
4C	00110010	9C	00111001	EC	00110111
4D	10110010	9D	10111001	ED	10110111
4E	01110010	9E	01111001	EE	01110111
4F	11110010	9F	11111001	EF	11110111
F0	00001111	F6	01101111	FB	11011111
F1	10001111	F7	11101111	FC	00111111
F2	01001111	F8	00011111	FD	10111111
F3	11001111	F9	10011111	FE	01111111
F4	00101111	FA	01011111	FF	11111111
F5	10101111				



Big BERT Display
Figure 3-19

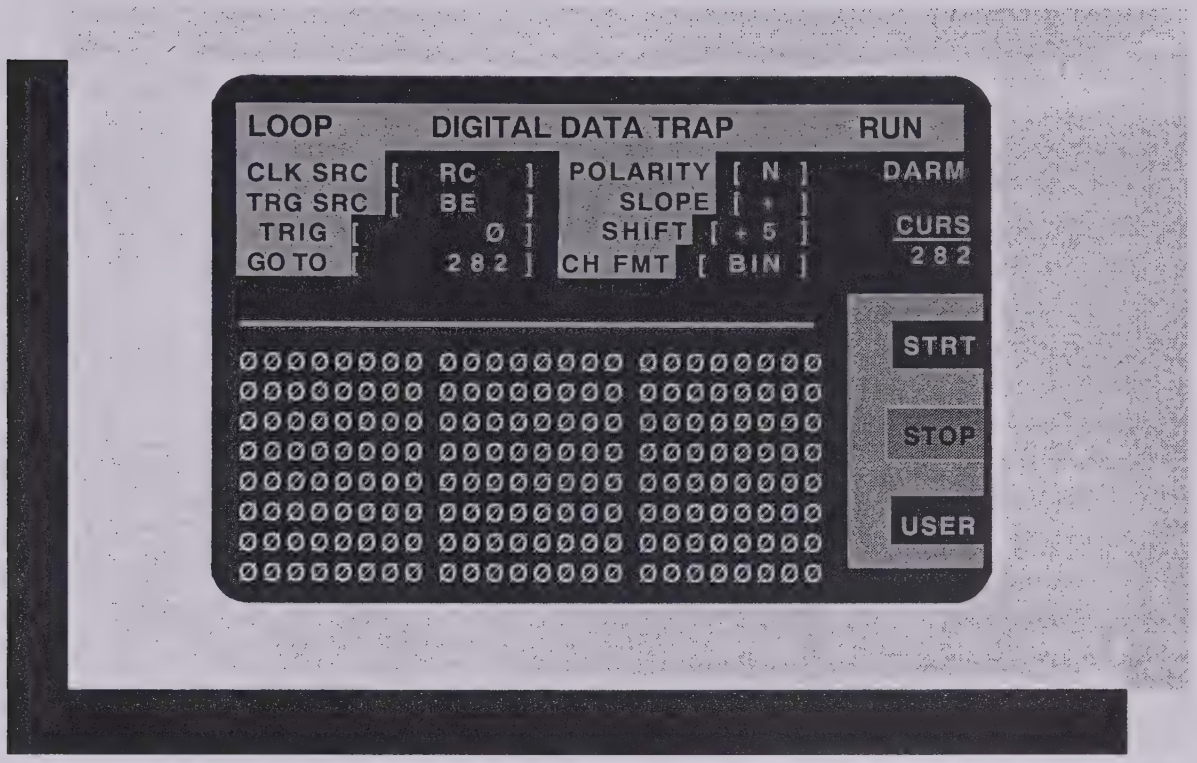
for display by using the UP/DOWN CURSOR keys to place the half intensity block in the top or bottom half of the display. Then, using the select keys, the user may scroll through any of the parameters being measured and display whichever one is desired.

> **NOTE**
>
> This does not interfere with the test in progress.

The BIG BERT display permits viewing any two parameters from a distance and is helpful when the test technician has to be some distance from the test set.

3.3.12 Digital Data Trap Menu

The Digital Data Trap menu, shown in Figure 3-20, is used to display the bit-by-bit history of a selected event in time. The softkeys associated with this menu are the START and STOP keys which, as the names imply, start and stop the trap mode and the USER/CAN key which is used to move the selected portion of the data that has been trapped into one of the four user patterns. By using this feature, the user is able to trap that portion of live traffic that is causing problems on a pattern sensitive network and use that pattern to test the network.



Digital Data Trap Display
Figure 3–20

NOTE

Obviously, any pattern could be trapped and placed into the user pattern for testing. This may result in a pattern that does not fall within the pattern sync criteria of the 5500A. If that is the case, the 5500A will **NOT** obtain pattern sync. However, the pattern may still be used for testing the network for problems other than pattern sync problems.

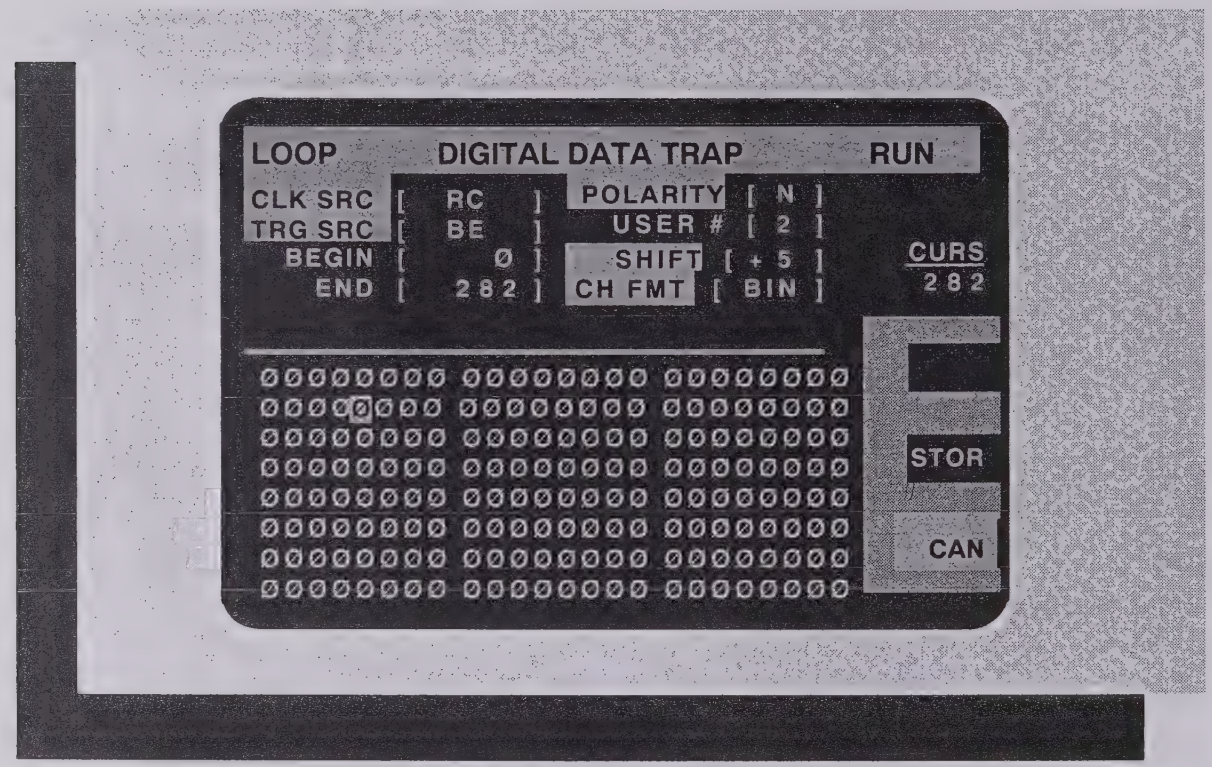
To use the data trap and user pattern feature, follow the steps below:

1. Set up the data trap to trap the desired portion of the signal being monitored. (for example, if frequent bit errors are the problem, you would set the bit trap to trigger on a BE).

2. After the data trap has "trapped" the desired segment of traffic, press the USER softkey.

3. The bit trap menu will change and appear as shown in Figure 3–21.

4. Select the user pattern number into which you wish to write the "trapped" pattern. Enter this number in the flashing field opposite USER # (2 in example shown).



Digital Data Trap Display After User Softkey is Pressed
Figure 3-21

CAUTION

Whatever user pattern (1 thru 4) is selected, the data in that location will be overwritten and lost when the "trapped" pattern is entered.

NOTE

Pressing the CAN softkey at any time while in this menu, will cancel all operations and return you to the main bit trap menu without storing a pattern in the user pattern memory.

5. Select the cursor location that marks the beginning of the pattern within the "trapped" data and enter that number in the flashing BEGIN field (0 in illustration shown).

6. Select the cursor location that marks the end of the pattern within the "trapped" data and enter that number in the flashing END field (282 in illustration shown).

7. Press the STOR softkey. This transfers the "trapped" pattern to the selected user pattern.

8. Verification of the pattern transfer may be accomplished by selecting USER PATTERN menu and viewing the pattern stored in the selected location.

The remaining lines on the main bit trap menu are as follows:

CLK SRC – The clock source is the receive clock. Future software enhancements may permit user selection of other clock sources.

TRG SRC – The trigger source is bit errors (BE). Future software enhancements may permit user selection of other trigger sources.

TRIG – The bit trap utilizes a 64,000 bit buffer. The user may insert a number, using the front panel keypad, between 0 and 63,992. That number is the location in the buffer where the trigger will be stored. This permits the user to view data before and after the trigger in the ratio best suited for the particular event/test.

GO TO – A number may be entered here from the front panel keyboard to place the cursor anywhere within the 64,000 bit buffer. The number may be any number between 0 and 63,999.

POLARITY – The polarity is a default setting to obtain optimum performance. The polarity line is on the menu to permit future software enhancements which may permit user selection of the trigger polarity.

SLOPE – The slope is a default setting to obtain optimum performance. The slope line is on the menu to permit future software enhancements which may permit user selection of the trigger slope.

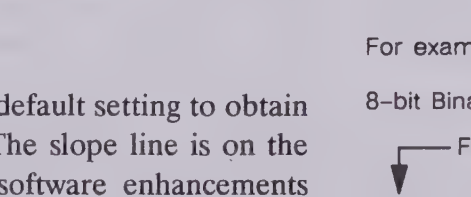
SHIFT – The user may shift the data bits being viewed on the screen from –8 to +8 bits. This also changes the LSB and MSB of the eight bit bytes and will change the HEX value of the bytes.

CH FMT – The user may view the data stored in the trap in either binary (BIN) or hexidecimal in (HXL or HXM).

The Digital Data Trap menu displays binary received data in the order that it was received relative to time, left–to–right, top–to–bottom, on the screen. The binary bit in the upper left corner was received first and the binary bit in the lower right corner was received last (the bit highlighted is the bit on which the bit trap triggered). The binary data is organized on 8–bit boundaries to facilitate conversion to hex data. The data may be shifted left or right 8 bits in either direction to group any consecutive 8 bits into 8–bit words. Since the binary data is displayed in the order it was received (left–to–right, top–to–bottom) the leftmost bit in each 8–bit boundary was received **first**, followed by the 7 bits immediately to its right. To convert the binary data to hex data, the user must select either HXL or HXM format in the CH FMT field on the display. HXL format defines the leftmost bit (first received) of each 8–bit word as the LSB (least significant bit) and creates a "LSB FIRST RECEIVED" hex word. HXM format defines the leftmost bit of each 8–bit word as the MSB (most significant bit) and creates a "MSB FIRST RECEIVED" hex word.

For example:

8–bit Binary word received as displayed:



Converts to HXL hex word = 50 LSB 1st

Converts to HXM hex word = 0A MSB 1st

To illustrate this point, take the case of the 5500A USER PATTERN. Data is entered into the user pattern in hex format. When a hex word is written as binary, the MSB is normally on the left and the LSB is normally on the right.

For example:

50 hex

0 1 0 1 0 0 0 0 binary
MSB LSB

When a user pattern hex word is transmitted, it is transmitted LSB FIRST. That is, the first bit transmitted of the hex word 50 would be a "0" followed by "0-0-0-1-0-1" followed by the MSB "0" transmitted last. When this byte is received and displayed in binary format by the Digital Data Trap, it would appear as:

0 0 0 0 1 0 1 0

because the first bit received is always displayed as the leftmost bit in each 8-bit word. The digital trap has no way of knowing whether the binary data it received arrived LSB FIRST or MSB FIRST. The trap only displays binary data in the order that it was received relative to time (left-to-right, top-to-bottom). It is up to the user to determine whether the MSB or the LSB of an eight bit byte was received first. In the above example, the LSB was received first. Therefore the user would select the HXL format to convert the binary data to hex, and display the received user pattern.

3.3.13 Other Menus

The optional displays (High Speed Jitter, MSU Configuration, etc.) are discussed in the applicable option instruction book. The G.821 performance monitoring menu is discussed in section 6, Performance Monitoring, of this instruction book.

3.4 FREQUENCY MEASUREMENT

The Model 5500A is also a frequency counter with a resolution of 0.1 HZ below 1 MHZ and 1 HZ above 1 MHZ. The reading is displayed on the main BERT menu as shown in Figure 3-10. The user may select BR to view the asynchronous Baud Rate, or TC (Transmit Clock), RC (Receive Clock) or XC (External Clock) in synchronous system testing.

The Model 5500A counter provides the user with a reasonably accurate diagnostic tool for uncovering frequency related error problems. This enables the user to spot a drifting clock. When the test set is set up in the EXT clock mode, the user can measure and determine the stability of the receive clock by selecting RC. When acting as a synchronous DTE it is convenient to check the outgoing clock by selecting TC. The user can easily compare the transmit and receive clocks for significant differences. When a USER clock input to the rear panel BNC connector has been selected the user can measure it on the TC of transmit clock field.

The user may measure the external clock (Pin 24 on the RS-232 interface module) signal by selecting XC. This would be used when the Model 5500A is deriving its clock from an external source such as a modem or terminal to time its transmitter.

Frequency counter display accuracy is a function of the stability of the internal 4.608 MHZ reference clock oscillator. The Model 5500A uses a software controlled correction to zero out the impact of the crystals in accuracy and so all that remains is the effect of thermal stability or drift. This is typically less than 5 parts per million with the standard crystal and can be reduced to 1 part per million or less with the precision clock (Model 5500A-CL01) option.

The software controlled calibration command for the frequency counter - TWEAK - is described in detail in section 4.9, REMOTE PROGRAMMING, NO TAG and the procedure for the TWEAK adjustment is found in section 5, the maintenance section, of this instruction book.

3.5 TIME MEASUREMENTS

3.5.1 Event Timing

The Model 5500A measures the time interval between transitions of any two selected interface signals (listed below) to 4.67 minutes duration with a resolution of 1 microsecond to 10 milliseconds depending upon scale.

RTS /	DTR /
RTS \	DTR \
RD /	DCD /
RD \	DCD \
TD	DSR /
TD \	DSR \
SQ /	CTS \
SQ /	CTS \

The "/" character after a signal indicates that signal going "TRUE". For an RS-232 interface, a MARK to SPACE (1 to 0) transition is the TRUE condition. The "\" character shows a transition to FALSE. On a TTL interface a "HIGH" to "LOW" transition is the TRUE condition. If an "I" is displayed, valid transitions have occurred, and an "I" for indeterminate is shown.

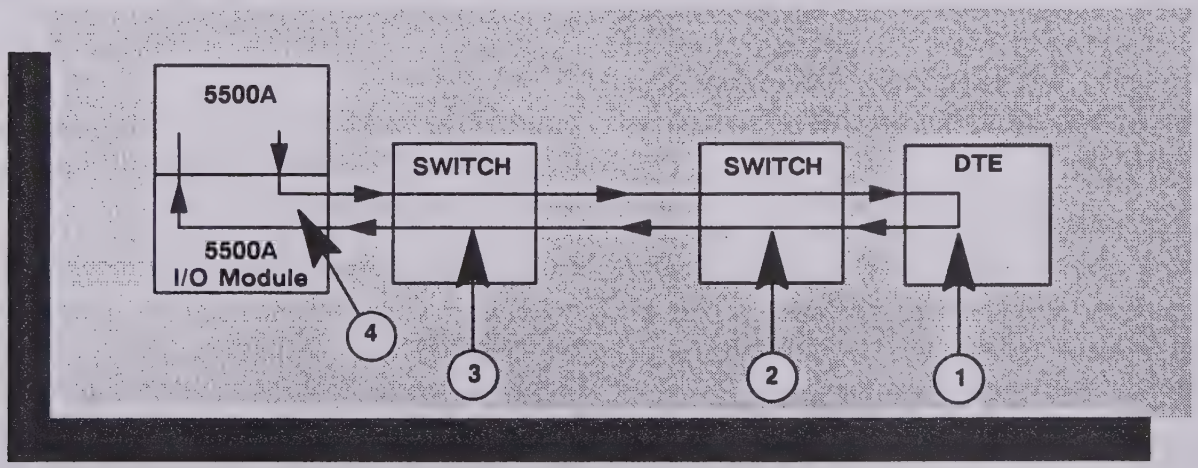
The user selects the resolution as 1us, 10us, 100us, 1MS, or 10MS, and then chooses which two events are to be measured. The Model 5500A automatically measures the time delay between the transitions, and updates the measurements display on a continuous basis.

3.5.2 Network Loop Timing

The 5500A is equipped with a network loop delay timer. The timer can operate while any of the pseudorandom patterns are being generated by the 5500A and looped back to the 5500A from some point in the network. An example is presented in Figure 3-22.

In the example shown, the 5500A is transmitting through some switches to a DTE. The DTE is set to loop the signal back (point 1) along the path to its source. In this configuration the 5500A will measure the total loop time for the entire path.

In the event the user desires to measure only parts of the path, a tare function is included with the timer circuit. Any section of the path that can be set to loop back can be subtracted from the total loop time. This subtracted time is referred to as the tare value. If, for example, a loop back was placed at position 4, the loop delay timer can be



5500A Network Loop Delay
Figure 3-22

set to tare the delay in the 5500A I/O module. Then when the configuration is returned to loop back at position 1, the delay inherent in the I/O module will be subtracted and the loop time which is displayed is the delay time contained in all of the network external to the 5500A.

In a similar manner, tare values could be established by looping the network at points 2 or 3 if it was desired to pin-point a delay to a particular circuit/component.

The network loop delay timer can measure times to 17 minutes and can display loop times in the following ranges of resolution; 1 usec, 10 usec, .1 Msec, 1 Msec, 10 Msec.

3.6 BIAS DISTORTION (SKEW)

The Model 5500A measures BIAS DISTORTION on the receive data lines. A pattern having a uniform 50/50 distribution of 1's and 0's is customarily used as the transmitted signal. Any of the Model 5500A pseudorandom sequences may be used.

Bias is determined as a ratio of MARKS (1's) to SPACES (0's) and expressed as a percentage.

A reading of 0% indicates a constant SPACE signal while a reading of 100% indicates a constant MARK signal. A 50% reading indicates ideal symmetry of MARK bit widths periods to SPACE bit widths periods.

A reading of 45% to 55% is considered acceptable in most systems. Some older modems may have larger windows of acceptable performance but in general readings outside the 45-55% range may be cause for further investigation.

If a modem or other device has filters shaping the bit stream, and they have degraded band pass characteristics which favor 1's over 0's or vice versa then the likelihood of an error occurring is increased.

Bias Distortion was more of a problem with older FSK type modems employing lumped element filters than it is with modern modems which use digital filter techniques.

Bias Distortion measurement accuracy is +1%, and the reading is updated at least once per second.

3.7 BER TEST ASSISTANCE

Table 3-7 presents a list of possible problem areas if the Model 5500A does not achieve synchronization with the device under test.

3.8 ACTIVITY INDICATORS

There are 12 green LED's on the 5500A front panel to indicate activity of the installed interface module.

The actual points being monitored are on the TTL interface between the module and control board. Since there are many different module options, all front panel indicators may not be applicable to a particular interface.

In addition, some of the indicators change meaning when modes are switched between DTE and DCE.

Tables 3-8 and 3-9 relate the LED's to the interface circuit being monitored, for each module and mode of operation.

The LED indicators provide interface activity status as well as mode (RUN), async, sync recovery and error injection status. These provide a quick visual indication of what is occurring at the interface and can often lead to rapidly identifying the source of a problem. For instance, if the Model 5500A is transmitting data and the TD LED is lit but there is no received data (RD LED not lit)

then it is possible that the transmission source at the distant end is not functioning. This could be a modem which is receiving data but whose transmit section has become defective.

Table 3–7. BER Test Assistance

PROBLEM	CORRECTIVE ACTION
SYNC LED does not illuminate	Verify that the data format and patterns in the BERT FORMAT menu are correct. Check bit rates, sync/async mode, character size, parity etc. Verify that correct mode (DCE or DTE) has been selected. Verify that correct mode (RTS/DCD) has been selected. Verify that BRIDGE mode in T–Carrier testing has not been selected. (BRIDGE mode disables the Model 5500A transmitter; however, the receive BERT test capability is fully functional in the BRIDGE mode as long as the selected BERT pattern is on the circuits and the transmission line is otherwise properly terminated.) Verify that item under test is not open circuited.
Continuous Bit Error Indicated	If two Model 5500A's are connected for end to end testing, make sure the bit rates, patterns, modes, etc. are the same in both units. Also, in SYNC mode, ensure that one unit supplies clock and the other is set to EXT clock.
SYNC LED blinks on and off in synchronous testing	If two test sets are operating in an end to end test verify that one is set to supply clock (internal timing) and the other is set to EXTERNAL clock. If a modem or other device in the circuit is the master clock, set both sets to external. Note: There can be only one Master Clock in a synchronous circuit.
SYNC LED not illuminated and TD LED is off	Verify that RTS is activated if unit is configured as DTE.
Constant bursts of errors detected in testing synchronous devices	Select External clock mode if not already selected. (Most synchronous devices are strapped to supply clock).
Test data does not accumulate	Verify RUN switch has been depressed and RUN LED is lit.

Table 3-7. BER Test Assistance

PROBLEM	CORRECTIVE ACTION
Test suddenly stops and RUN LED goes off.	If continuous testing is desired verify that "00:00:00" has been placed in the test time window and press RUN. If testing for a specific time, verify that the time selected has elapsed when set stops. This is normal operation.
5500A displays errors with T1 module installed	Verify that QRW pattern has been selected instead of a pattern without > 14 zero suppression. Verify equipment under test has zero suppression enabled. Verify that error rate is above acceptable levels. Note that T1 carrier systems are only specified to provide a 1x10-6 error/bit rate which is about three errors or less every two seconds.
RAM error on power-up	Battery may be discharged. Leave power on unit for 24 hours to charge up battery.

Table 3-8. RS-232/RS-449 Activity Indicators.

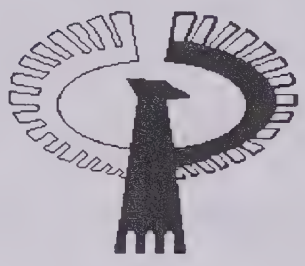
INDICATOR	ACTIVITY			
	RS-232		RS-449	
	DTE	DCE	DTE	DCE
TD/RD	Xmit Data	Rx Data	Send Data	Receive Data
RD/TD	Rx Data	Xmit Data	Receive Data	Send Data
RC/RC	Rx Clock	Rx Clock	Receive Timing	Receive Timing
TC/TC	Tx Clock	Tx Clock	Xmit Timing	Xmit Timing
RTS/DCD	Request to Send	5500A Data Carrier Det.	Request to Send	Receive Ready
CTS/RTS	Clear to Send	Clear to Send	Clear to Send	Request to Send
DSR/DTR	DSR	DTR	Data Mode	Terminal Ready
DTR/DSR	DTR	DSR	Terminal Ready	Data Mode
DCD/CTS	Data Carrier Det	Clear to Send	Receiver Ready	Clear to Send
RI/RI	Ring Indicator	Ring Indicator	Incoming Call	Incoming Call
SQ/SQ	Signal Quality	Signal Quality	Signal Quality	Signal Quality
SCTE/SCTE	SCTE	SCTE	Terminal Tim	Terminal Tim

Table 3-9. T1/T1C and V.35 Activity Indicators.

INDICATOR	ACTIVITY			
			V.35	
	T1/T1C	Framed T1	DTE	DCE
TD/RD	Xmit Data	Xmit Data	Xmit Data	Receive Data
RD/TD	Receive Data	Receive Data	Receive Data	Xmit Data
RC/RC	Recovered Receive Clock	Gated Internal Clock	Element Timing Xmit Signal	Element Timing Xmit Signal
TC/TC	Recovered Xmit Clock	Gated Internal Clock	Element Timing	Element Timing Data Chann Rec
RTS/DCD	X*	X*	Request to Send	Line Signal Det
CTS/RTS	X	N/A	Ready for Sending	Request to Send
DSR/DTR	X	X	Data Set Ready	Data Terminal Ready
DTR/DSR	X*	X	Data Terminal Ready	Data Set ready
DCD/CTS	X	X*	Receive Data Channel Receive Line Signal Detector	Drive ready for Sending
RI/RI	X	X	Calling Indicator	Calling Indicator
SQ/SQ	X	X	X	X
SCTE/SCTE	Internal Clock Source	Gated Recovery Receive Clock	Transmitter Signal Element Timing (DTE Source)	Transmitter Signal Element Timing (DTE Source)

* May be control signals pertinent to internal 5500A functions on these monitored lines.

5500A Telecommunications Analyzer



Phoenix

Remote Operation – Section 5

Initial Setup, Electrical Connection, Command Descriptions, and Big Screen Display.

34–00057–115TB
1st Edition, 1 Feb 1989
1st Revision, 15 September 1989, Change 1, 1 Jan 1990

table of contents

Paragraph		*Page #*
5.0	INTRODUCTION	5–1
5.1	INITIAL SETUP	5–1
5.2	ELECTRICAL CONNECTION	5–3
5.2.1	RS232 Port	5–3
5.2.2	IEEE–488 Port	5–3
5.3	COMMAND DESCRIPTION	5–3
5.3.1	System Commands	5–4
5.3.2	Printer Commands	5–4
5.3.3	Event Timing Commands	5–21
5.3.4	User Programs, Patterns, and Sequence Commands	5–23
5.3.5	BERT Setup Commands	5–24
5.3.6	BERT Result Commands	5–30
5.3.7	Low Speed Jitter	5–33
5.3.8	Other Remote Commands	5–33
5.4	REMOTE "BIG SCREEN" DISPLAY	5–33

List of Figures

Title	*Figure #*	*Page #*
Model 5500A Remote Configuration Menu	Figure 5–1	5–1
Model 5500A Main Help Menu – Screen 1	Figure 5–2	5–5
Model 5500A Main Help Menu – Screen 2	Figure 5–2	5–5
Model 5500A Main Help Menu – Screen 3	Figure 5–2	5–6
Model 5500A Main Help Menu – Screen 4	Figure 5–2	5–6
Model 5500A Main Help Menu – Screen 5	Figure 5–2	5–7
Model 5500A Main Help Menu – Screen 6	Figure 5–2	5–7
Model 5500A Main Help Menu – Screen 7	Figure 5–2	5–8
5500A Remote "Big Screen" Display – Page 1	Figure 5–3	5–34
5500A Remote "Big Screen" Display – Page 2	Figure 5–3	5–35
5500A Remote "Big Screen" Display – Page 3	Figure 5–3	5–36

List of Tables

Table # ..... *Title* ..... *Page #*

Table 5–1. ..... Model 5500A Remote System Commands. 5–9

Table 5–2. ... Model 5500A Remote Event Timing Commands. 5–22

Table 5–3. Model 5500A Remote User Programs and Patterns Commands. 5–23

Table 5–4. ... Model 5500A Remote BERT Setup Commands. 5–24

Table 5–5. ... Model 5500A Remote BERT Results Commands. 5–30

List of Effective Pages

* 0 in this column indicates original page

Page No	*Change No	Page No	*Change No	Page No	*Change No
5-1 to 5-2a	1				
5-2b	Blank				
5-3 to 5-36	0				

RECORD OF CHANGES

CHANGE NUMBER	CHANGE DATE	CHANGE NUMBER	CHANGE DATE	CHANGE NUMBER	CHANGE DATE
Preliminary	11/88				
1st Edition	2/89				
1st Revision	9/89				
Change 1	1/90				

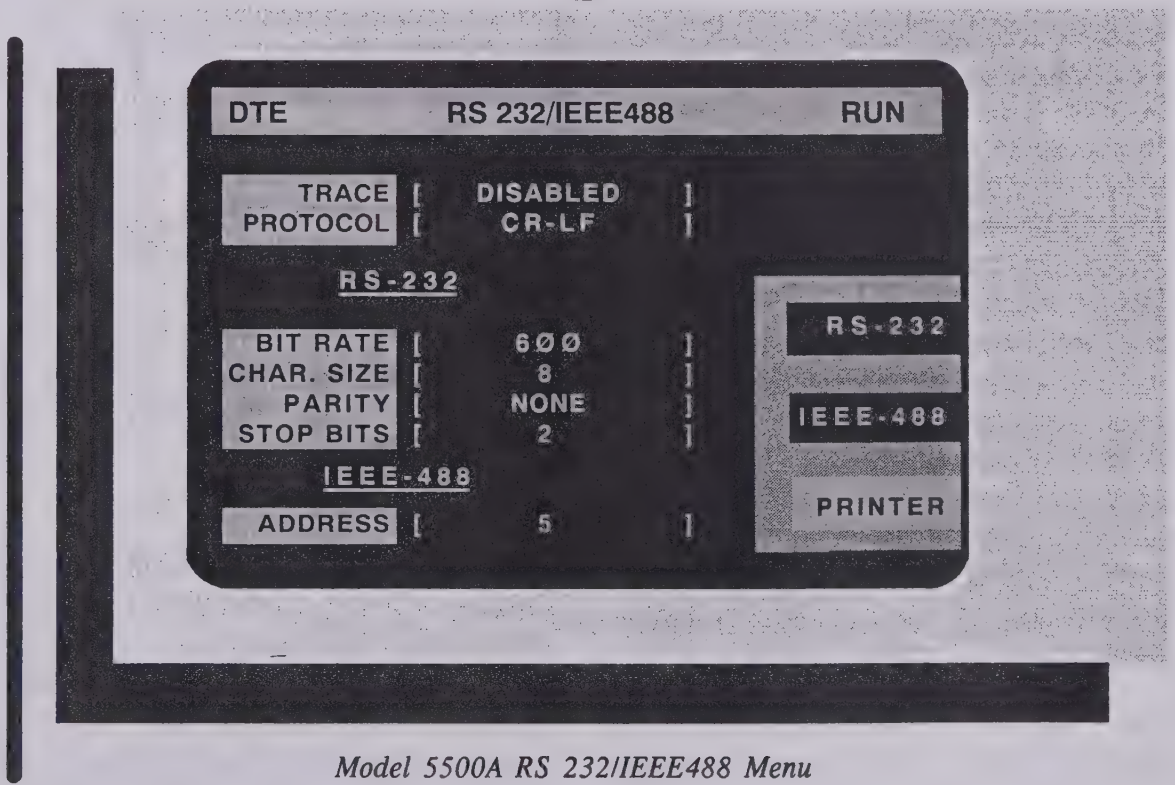
remote operation

5.0 INTRODUCTION

The Model 5500A remote control ports permit the user to control the 5500A from a computer or dumb terminal. Both IEEE–488 and RS–232 ports are provided. Both connectors are located on the rear panel of the 5500A. Before connecting the 5500A to one of the remote ports, the remote port must be selected and the remote port characteristics must be configured to match the computer or terminal characteristics.

5.1 INITIAL SETUP

Select the RS 232/IEEE488 menu on the Model 5500A (refer to Figure 5–1). This menu is used to configure the 5500A to match those of the terminal or computer to be used as the remote control device. Enabling the TRACE on the menu permits the user to monitor the character data streams across the RS–232 bus. Data from the terminal will appear on the left of the screen on the second line from the top (line with the "] [" in the center) while the data from the 5500A to the



Model 5500A RS 232/IEEE488 Menu
Figure 5–1

communicating device will appear on the same line to the right.

The 5500A supports four modes of protocol:

1. IEEE488 CR-LF
2. IEEE488 ACK
3. RS232 CR-LF
4. RS232 ACK

a) IEEE-488/CRLF

1. Install the GPIB card in your computer and configure the software as described by National Instruments installation procedure.
2. Run "IBCONF" on your computer and change the configuration of "GBIB0" as follows:

Primary GPIB Address	0
Secondary GPIB Address	NONE
Timeout Setting	T10s
EOS Byte	0DH
Terminate Read on EOS	NO
Set EOI with EOS on Write	YES
Type of compare on EOS	7-bit
Set EOI with last byte of write	NO
GPIB-PC Model	PC2
Board is System Controller	YES
Local Lockout on all devices	YES
Disable Auto Serial Polling	YES
Disable Device Unaddressing	NO
High Speed Timing	NO
Interupt Jumper Setting	NONE
Base I/O Address	(2B8H)
DMA Channel	NONE
Internal Clock (in MHZ)	8

When the controller (PC) is configured as a talker (TE) and the 5500A is configured as a listener (LE), an absolute terminator <CR> carriage return will be sent by the talker. For example, <COMMAND> <CR>, the EOS byte will be sent by the talker along with EOI to the listener. The listener (5500A) recognizes that this is a command and will respond accordingly. Do not attempt to terminate commands with characters other than a <CR> as unperdictable results may be experienced.

3. Configure the 5500A as devices in "IBCONF". The recommended setup is as follows:

Primary GPIB Address	<user defined>
Secondary GPIB Address	NONE
Timeout Setting	T10s
EOS Byte	0DH
Terminate Read on EOS	NO
Set EOI with EOS on Write	YES
Type of compare on EOS	7-bit
Set EOI with last byte of write	NO

Note that when the 5500A is configured as a talker (TE) and the controller (PC) is configured as a listener (LE) that the 5500A now sends a **unique** terminator with EOI, i.e., <RESPONSE> CR LF 00H. This unique terminator is a null character (00H) and is reflected by a "Z" character in the trace display on the 5500A. False terminators have been experienced with certain IEEE488 controllers because we have embedded <LF> throughout our response messages. Therefore it was necessary to create an unique terminator. This protocol is only valid with software revision 7.04 or higher.

b) IEEE-488/ACK

Unlike the previous mode, in which the controller operated in an open loop manner, the ACK protocol provides a response to each command regardless of whether the command returns data. If the command is understood an ACK (06H) character is returned. If an error is encountered in interpreting the command, NAK (15H) is returned. If ad-

ditional data is to be returned it follows the first ACK and is terminated by a second ACK. Three possible responses are shown below:

(error)	NAK	EOI
(good, no data)	ACK	EOI
(good, data)	ACK	
	Char 1	
	"	
	"	
Char x		
ACK	EOI	

In all cases the EOI line indicates end of response.

c) RS232/ACK

Operation of the RS-232/ACK protocol is identical to the IEEE-488 protocol with the exception that there is no EOI line. It is the controllers responsibility to know whether or not additional data is expected following the first ACK. In practice this knowledge comes naturally with the program organization.

This protocol uses a half duplex data transfer structure on the RS232 port. The Model 5500 controls data flow to itself through the DTR line and sends data via the RTS/CTS handshake.

d) RS232/CRLF

This mode is intended primarily for use with a directly connected terminal. It operates full duplex and echoes every character received. In this mode, DEL and <Back Space> send a character sequence, the response to which will delete the last character. A <Control X> will cause the Model 5500 to ignore the present line. If an error is encountered in interpreting the input line, it is reprinted to the error point and a question mark (?) is inserted. The response to the command is shown on the line following the command.

When a protocol has been selected, use the cursor movement, cursor select keys, and softkeys to make the Remote Port Configuration menu, as shown in Figure 5-1, match the selected characteristics. In the example shown in Figure 5-1, RS232 has been selected by pressing the top

THIS PAGE LEFT INTENTIONALL BLANK

Index

Page Numbers in *Italic* indicate *Figure*
Page Numbers in **Bold** indicate **Warning**, **Caution**, or **Note**

A

Accessories, 1-1
Acronyms, 1-2
Activity Indicators, 3-54
Automatic Resync, 3-22

B

BER Test Assistance, 3-54
BERT Parameters, Definitions, 4-2
% Frame Bit Error Free Seconds (FFS%), 4-7
%CRC Error Free Seconds (CFS%), 4-5
15 Zero Seconds (15ZS), 4-10
15 Zeros (15Z), 4-10
Adjusted Bit Error Rate (ABER), 4-2
Adjusted Bit Errors (ABE), 4-2
Alarm History (AHST), 4-3
Alarms (ALRM), 4-2
Bit Error Rate (BER), 4-3
Bit Errors (BE), 4-3
Blocks (BLK), 4-4
Blue Alarm Seconds (BALS), 4-3
Burst Errors, 4-4
Clock Slip (CSLP). *See* Loop Timing
CRC Error Free Seconds (CEFS), 4-5
CRC Error Rate (CRER), 4-5
CRC Errored Seconds (CRES), 4-5
CRC Errors (CRCE), 4-4
Current Bit Error Rate (CBER), 4-4
Current Bit Errors (CBE), 4-4
Elapsed Time (ET), 4-6
Elapsed Time in Seconds (ETS), 4-6
Error Free Blocks (EFB), 4-5
Error Free Seconds (EFS), 4-6
Errored Block Rate (EBR), 4-5
Errored Blocks (BLE), 4-4
Errored Days (ED), 4-5
Errored Second Rate (ESR), 4-6
Errored Seconds (ES), 4-6
Frame Bit Error Free Seconds (FEFS), 4-7
Frame Bit Error Rate (FBER), 4-7
Frame Bit Errored Seconds (FBES), 4-7
Frame Bit Errors (FBE), 4-6
Frame Loss Seconds (FLS), 4-7
Frame Sync Loss (FLOS), 4-7
Loop Timing, 4-7
Loss of Sync (LOS), 4-8
Month/Day/Year (MDY), 4-8
Pattern Slips (PSL+/-), 4-9
Percent Error Free Seconds (EFS%), 4-6
Percent One's Density (%1sD), 4-6
Power Failures (PF), 4-9
Receive Bipolar Violations (RBPV), 4-9
Receive Violation Free Seconds (RVFS), 4-9
Receive Violation Rate (RVR), 4-9
Receive Violation Seconds (RVS), 4-9
Received Data Bits (BITS), 4-4
Slip Rate, 4-8
Sync Loss Seconds (SLS), 4-9
Time of Day (TOD), 4-10
Transmit Bipolar Violations (TBPV), 4-9
Transmit Violation Free Seconds (TVFS), 4-10
Transmit Violation Rate (TVR), 4-10
Transmit Violation Seconds (TVS), 4-10
Wander, 4-8
See also Loop Timing
Yellow Alarm Seconds (YALS), 4-10

Bias Distortion, 3–54
BIT Trap, 3–48
Bridge Mode, 3–23

C

Calibration, 7–2
  Control Board, 7–5
  Power Supply
    Emergency, 7–4
    Normal, 7–2
  Video Control Board, 7–7
    Intensity Adjustment, 7–9
CAUTION, User Pattern Overwrite, **3–50**
Connectors, Rear Panel, Power Cord
    Connection, 3–7
Controls
  Front Panel, 3–1
    Cursor, 3–2
    DCE/DTE Toggle Switch, 3–4
    DTR/DSR Toggle Switch, 3–4
    Help, 3–4
    Keypad, 3–3
    Menu, 3–2
    Recall, 3–4
    RTS/DCD Toggle Switch, 3–4
    Run/Stop, 3–1
    Select, 3–2
    Softkeys, 3–3
    Store, 3–4
  Rear Panel, 3–7
    Brightness. *See* Adjustments
    main power, 3–7
    main power select, 3–7
Controls and Indicators
  Front Panel, *3–6*
  Rear Panel, *3–11*
Customer Service Department, 2–6

E

Equipment Supplied, with 5500A, 1–1
Event Timing, 1–5

F

Frequency Measurement, 3–52

I

Identification Plate, 3–9
IEEE–488 Remote Port, location, 3–9
Indicator, Front Panel
  Error Injection, 3–4
  Interface Activity, 3–5
  Run, 3–3
  Sync, 3–4
  Sync Rec, 3–4
Initial Power Up, 3–12
Instruction Book, 1–3
Interface Options, 1–1

L

Loop Timing, 4–7

M

Main Power Fuse, Location, 3–7
Main Power Selection, location, 3–7
Main Power Switch, location, 3–7
Menu, 3–13
  5500A Configuration, *3–13*, 3–14, *3–15*
  BERT Setup
    RS–232
      Bit Rate, 3–18
      Blocks, 3–21, 3–25
      Character Size, 3–20
      Clock Invert, 3–18
      Data Invert, 3–18
      DCE SYN TD CLK, 3–20
      DTE/DCE, 3–18
      Error Inject Rate, 3–22
      Mode, 3–20

Parity, 3-20
Pattern, 3-20
Stop Bits, 3-20
TOD, 3-18
T1
Auto Resync, 3-28
Bit Rate, 3-24
Block Size, 3-21, 3-24
Blocks, 3-21, 3-25
Clock Source, 3-27
Frame, 3-24
Line Code, 3-24
Logic Error Injection Rate, 3-27
Pattern, 3-24
Test Time, 3-21
Test Time/Blocks, 3-24, 3-25
TOD, 3-24
TX ENA BDG/MON, 3-29
BERT Results/Parameters, 3-30
ESF T1, 3-33, *3-34*
RS-232, 3-30, *3-31*
BERT Setup, 3-17
RS-232, 3-18, *3-19*
Big BERT, 3-45, *3-48*
BIT Trap, 3-48, *3-49*
Graph Display, 3-38, *3-39*
Graph Setup, 3-36, *3-37*
Help, *3-14*
Help, 3-13
Softkey, 3-13
Printer Setup, 3-33
ESF T1, *3-36*
RS-232, *3-35*
RS 232/IEEE488, *3-42*
See also Remote Setup
RS-232 BERT Setup, *3-12*
Store/Recall Setups, 3-42, *3-43*
5500A Configuration, *2-4*, *3-16*
T1 ESF BERT Setup, T1, 3-22, *3-23*
User Pattern, *3-44*, 3-44

Monitor Mode, 3-23

N

network loop delay. *See* loop delay

NOTE
CAN softkey, Bit trap menu, **3-50**
DCE connects to DTE, **2-4**
Graph Data Buffer, size, **3-41**
pattern sync, with trapped user pattern, **3-49**
print resolution, **5-19**
screen response delays, **5-4**
T1 Bert Setup, Softkeys, **3-23**
T1 Error Inject, with 5500-628 module, **3-25**
User Pattern
interference with test, **3-48**
Set Code, **3-45**
User Pattern FAIL, battery fail, **3-44**

O

Options
See also accessories
Descriptions, 8-2
Bell 303 (5500-900), 8-5
Bi-Phase (5500-605), 8-3
DDS (5500-538), 8-3
DS-1/DS-1C (5500-600), 8-3
DS0/DS0A (5500-539), 8-3
DS1(T1) (5500-628), 8-3
G.703 2.048 Mbps (5500-815), 8-4
G.703 2.048 Mbps (5500-828), 8-5
G.703 64 kbps (5500-810), 8-4
G.703 8448 kbps (5500-805), 8-4
Jitter, 8-5
5500-JO2 High Speed T1, 8-5
5500-JO5 High Speed G.703 2.048 Mbps, 8-5
MSU Control Module (5500-555), 8-3
RS-232 (5500-200), 8-2
RS-499 (5500-450), 8-2
T2 (5500-700), 8-4
TTL (5500-500), 8-3
V.35 (5500-300), 8-2

Part Numbers, 8–1

P

Power Selection, 50/60 Hertz, 2–3

PROM, Replacement, 7–1

R

Remote Control
  Command Description, 5–3
    BERT Result Commands, 5–30
    BERT Setup Commands, 5–24
    Event Timing Commands, 5–21
    Printer Commands, 5–4
      PEND, 5–5
    Sequence Commands, 5–23
    System Commands, 5–4
    User Pattern Commands, 5–23
    User Program Commands, 5–23
  Electrical Connection
    IEEE–488 port, 5–3
    RS–232 port, 5–3
  Initial Setup, 5–1
    IEEE–488/ACK protocol, 5–2
    IEEE–488/CRLF protocol, 5–2
    RS–232/ACK protocol, 5–2a
    RS–232/CRLF protocol, 5–2a
  Other Commands, 5–33

Remote Port, Configuration, 2–4

Remote Setup, remote configuration menu, *5–1*

Resync, Auto, 3–22

Returning Merchandise
  Obtaining RMA number, 2–6
  Packing for, 2–5

RS–232 Remote/Printer Port, location, 3–9

S

Safety Summary, 2–1

Screen Saver, 2–3

Serial Number, location, 3–9

Softkeys
  BERT Setup Menu
    ESF T1, 3–22, 3–33
    RS–232, 3–18, 3–30
  Graph Setup Menu, 3–36
  Help Menu, 3–13
  Printer Setup Menu, 3–33
  RS–232/IEEE488 Menu, 3–41
  5500A Configuration Menu, 3–14
  Store/Recall Setups Menu, 3–42

Specifications, 1–3
  display, 1–7
    menus displayed, 1–7
  environmental, 1–7
  power requirements, 1–7
  rear panel connectors, 1–6
    IEEE–488, 1–6
    Interface, 1–6
    RS–232, 1–6
    User clock, 1–6
    video, 1–6
  rear panel test points, 1–6
  receiver, 1–4
    data error analysis, 1–4, 1–5
      calculated, 1–5
      G.703, 1–5
      numeric results, 1–5
      time dependent, 1–5
    timing, 1–4
  transmitter, 1–3
    pattern generator, 1–3
    timing sources, 1–4

T

T1–BERT
  Clock Slip, LTMD, 3–33
  Frequency, 3–33

Terminate Mode, 3–23

Test Points, Rear Panel, 3–8

Testing, Bit Error Rate, 4–1

Time Measurements
  Event Timing, 3–53

Network Loop Timing, 3-53

U

Unpacking and Inspection, 2-1
User Clock Jack, location, 3-9

V

Video Out Jack, location, 3-9

W

WARNING, input power, **2-3**
Warranty, 2-5

95915